MACRO

Motion And Control Ring Optical

The Light Link in Motion...

MOTION AND CONTROL RING OPTICAL

SPECIFICATION

PRELIMINARY

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ABSTRACT
The increasing needs of the machine control industry dictate a requirement for a simple high bandwidth data interface. MACRO (Motion And Control Ring Optical), a non-proprietary interface, satisfies growing needs for noise free data links between machine controllers and machine equipment cabinets that may reach as far as 10,000 feet.

MACRO is a communications standard for distributed machine control -- both motion and I/O.

MACRO uses a ring topology to allow master controllers to communicate with slave nodes and other master controllers.

1.0 Introduction

1.1 Overview

MACRO is organized as a ring of masters and slaves, a high-frequency real-time communications system with a bandwidth that is appropriate for multiple-axis precision motion control and tasks such as relay and valve control.

A MACRO network is connected using a ring topology; stations in the ring communicate through each other. There is no specified order in which masters and slaves are placed in a MACRO ring, therefore both master and slave stations on the ring pass through data that is not addressed to them.

The parallel nature of MACRO makes it as easy for a master to send command data, whether motor torque, motor velocity, or discrete outputs, across the ring to a remote node. Hardware systems that use registered data may be configured so as to communicate through MACRO. These systems include devices such as digital-to-analog converters (motor torque, motor velocity), or discrete output lines (relay control, valve control). Similarly, MACRO makes it easy for a master to read feedback data, such as motor position or discrete inputs, from a remote node. These systems include devices such as encoder counters or discrete input lines such as A-D converter inputs or switches.

1.2 Description

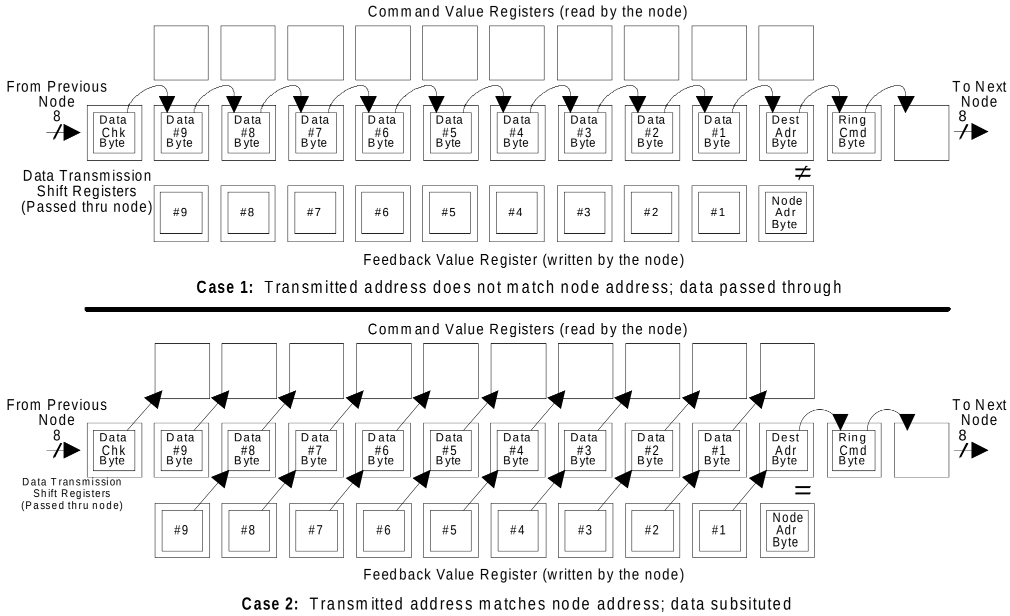
Communications throughout the ring is started by a pre-designated ring-master. This takes place at a fixed frequency (usually user-defined). For each ring communications cycle, each master on the ring sequentially sends a packet of data to each of its slaves, and receives feedback data from each of its slaves. Since masters always originate communications, slaves respond to master communications by substituting a response data packet in place of their command data packet into the communications stream.

A slave may only originate ring activity if the slave detects a ring break directly upstream. A ring break is observed by a slave when the first slave after the break determines that there is no ring activity. When this occurs the slave becomes responsible to start ring activity and sends a message that declares a ring break.

In a MACRO network design the data transmission across the ring is typically transparent to the software running at either end (master or slave). A set of data registers for input and output exist at both master and slave stations for any active node on the ring. For a master to send command data to a slave, data gets deposited to the proper output registers (command data) in the master's MACRO interface.

When activated, a master's ring hardware shifts all active node data from the master's transmit registers across the ring to matching input registers of the appropriate slave node. The slave's ring hardware shifts node data that is addressed to it into a set of receive registers. Data is returned into the ring at the same time that the data is received from the ring by the slave's hardware transmit registers.

A slave sends feedback data to its master by placing data into its ring hardware output registers. When the master transmits data to a specific slave, the ring hardware in the slave substitutes its transmit register information back into the ring at the same master/slave node address.



Note

It is not a requirement of MACRO that data transmission be handled directly in hardware. Due to the very high frequencies at which data transmission occurs, software involvement in MACRO ring transmissions is undesirable.

At the bit and byte level, communications are based on an encoding scheme originally developed for Fiber Distributed Data Interface (FDDI), which sends a self-clocking data stream with error checking encode/decode. This protocol has been implemented in the TAXIchip™ ICs from Advanced Micro Devices, and compatible ICs from other vendors. These aspects of the MACRO standard can be met by using the TAXIchip or equivalent ring transmitter and receiver ICs.

1.3 Glossary of MACRO Terms

Active Node: A node on the ring, master or slave, that is “turned on” to be able to transmit new data packets.

Baton: The signal between master stations on a ring that passes master control of the ring to the next master. Each master station transmits the baton signal to the next master downstream when it is done sending all of its command data packets.

Broadcast: The act of sending a data packet to multiple MACRO stations. The stations that receive the packet have an inactive broadcast node and retransmit the data back into the ring.

Broadcast Node: An inactive node that is usually intended to appear at more than one MACRO station. The stations that receive the packet have an inactive broadcast node and retransmit the data back into the ring.

Data Packet: The set of data that is transmitted or received by a node during each ring communications cycle. The MACRO protocol specifies this to be a 12 byte package.

Inactive Node: A node on the ring that is "turned off". This node is unable to retransmit new data packets. An inactive node may receive a data packet for monitoring and must re-transmit the data packet (broadcast node).

MACRO Ring Network: A system of devices that are interconnected by a fiber optic or twisted pair copper cable that uses MACRO protocols.

Master: An entity on the ring that sends command data packets and receives feedback data packets.

Master Node: A logical unit and set of registers on the ring that can send command data packets to a corresponding slave node, and receive feedback data packets from the corresponding slave node.

Master Number: A value from 0-15 that is assigned to each master node on a ring. The master number is used with the slave number to associate data packets with nodes.

Master Station: A station on the ring containing one or more master nodes.

Node: A logical unit on the ring. A node device sends and receives a data packet once each ring communications cycle. All nodes possess both a master number (0-15) and a slave number (0-15), whether the node is a master node or a slave node. For communications, there must be corresponding master and slave nodes.

Node Address Byte: The element of the MACRO data packet that contains both a master number (0-15) and a slave number (0-15). All MACRO data packets have this address header attached to them.

Ring Communication Cycle: A term that applies to the complete set of packets that are transmitted from the first synchronizing master through to the last node of the last master station on a ring.

Slave: An entity on the ring that receives command data packets and sends feedback data packets.

Slave Node: A logical unit and set of registers on the ring that can receive command data packets from a corresponding master node, and transmit feedback data packets back to the corresponding master node

Slave Number: A value from 0-15 associated with each node. There are 16 slave nodes which may be addressed per master in a ring. The slave number is used with the master number to associate data packets with nodes.

Slave Station: A station on the ring containing one or more slave nodes.

Source Master: A master station on the ring that initiates type 1 master to master communication to a target master.

Station: A physical unit on the ring with a ring receiving circuit, and ring transmission circuit, and the circuitry for one or more nodes. There may be more than one station in a single hardware device.

Station Delay: The amount of time it takes for data to pass through a single station. Some devices may contribute more than one station delay to a MACRO ring.

Sync Byte: A byte sent across the ring when no real data is being sent, in order to keep the ring clocks properly synchronized.

Synchronizing Master: The single master station on the ring that starts a ring communications cycle based on its own internal timing circuitry. Any other master stations on the ring must await receipt of the baton signal from the upstream master before starting its communications.

Target Master: A master station on the ring that receives type 1 master to master communication from a source master.

1.4 Definition of MACRO Compatibility

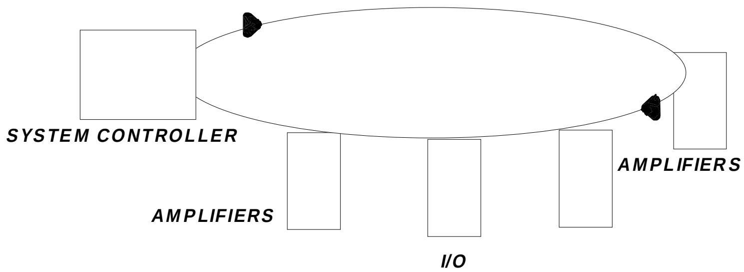
A device shall be considered MACRO compatible if it is capable of interconnecting with other MACRO devices that conform to the physical and logical requirements as described in this specification.

MACRO is intended to be an open architecture where different components that are MACRO compatible may coexist and operate with each other.

2.0 Network Organization

2.1 MACRO Ring Network

A MACRO ring network consists of a group of master and slave stations.



2.2 MACRO Stations

Each MACRO station shall have a single ring output and a single ring input. The output of one station is connected to the input of the next station, forming a ring topology.

There shall be at least one station that is a synchronizing master in a MACRO ring. This station contains one or more master nodes. This station may also contain one or more slave nodes.

A single station may contain any combination of both master nodes and slave nodes. There may be more than one MACRO station in a single hardware device.

2.2.1 Master Station

A master station shall handle data according to the following criteria:

1. Start to transmit data packets at receipt of the baton (CMD-1 twice) signal.
2. Transmit data packets for each of its active nodes.
3. Transmit at least one sync byte (CMD-0) between each active node packet.
4. Latch data feedback packets for each of its active nodes.
5. Latch inactive data packets (for inactive monitoring) and retransmit their data.
6. Retransmit any data packets not addressed for this master node.
7. Retransmit sync bytes (CMD-0) as they are received.
8. Transmit a baton signal (CMD-1 twice) when finished transmitting active nodes.

2.2.2 Synchronizing Master Station

The synchronizing master station shall be the master station in a ring that initiates ring operation.

This station shall start transmitting its active node packet data based upon a fixed time interval.

The minimum time interval for a ring cycle to be started by the synchronizing master shall be 1mS (1KHz). This time interval shall be of unchanging length during the operation of the MACRO ring.

NOTE
A common value for the synchronizing master to start transmission on the MACRO ring is 100µS (10 KHz).

A synchronizing master station shall handle data according to the following criteria:

1. Transmission for active data node packets is started based upon a fixed time interval.
2. Transmission of data occurs per the criteria described in Master Station above.
3. There shall be only 1 synchronizing master station attached to a MACRO ring.

2.2.3 Slave Station

A slave station shall handle data according to the following criteria:

1. Latch data command packets for each of its active nodes and substituting feedback packets back onto the ring.
2. Latch inactive data packets (for inactive monitoring) and retransmit their data.
3. Retransmit any data packets not addressed for this slave node.
4. Retransmit sync bytes (CMD-0) as they are received.
5. Retransmit the baton signal (CMD-1 twice) as it is received.

2.3 MACRO Nodes

A node is the basic logical unit on the ring. A node sends and receives a data packet during each ring communications cycle. The data packet in a node shall be fixed length of 9 bytes.

Typical node hardware shall have 4 input registers and 4 output registers. In each node there shall be one 24 bit (3 bytes) word, and three 16 bit (2 bytes) words. The data in a node shall be transmitted in ascending order starting with register 0.

Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Master Data Sent	Register 3	Register 2	Register 1	Register 0
Slave Data Returned	Register 3	Register 2	Register 1	Register 0

In a master node, the output registers contain command data written by the local station's processor and transmitted over the ring as command data packets. The input registers contain feedback data received from a corresponding slave node, which is read by the local station's hardware.

In a slave node, the output registers contain feedback data written by the local station's hardware and transmitted over the ring as feedback data packets. The input registers contain command data received from a corresponding master node, which is read by the local station's hardware.

Nodes on a station may be inactive. Inactive nodes shall "listen" (latch in data packets), but not change data. The inactive node station shall re-transmit that node's incoming data packets as if they were not addressed to the inactive node station.

2.4 Node Addressing (Binding the Ring)

The first byte of the MACRO data packet shall be the Node Address Byte. This byte shall contain 4 bits that select the master and 4 bits that select the slave address.

Every node on a MACRO ring shall have an 8-bit address number. The primary ring communications takes place between active master nodes and active slave nodes having the same address number.

There shall be only one active master node and one active slave node on the ring with any given address number. Since there are 256 possible address numbers, there may be 256 active master nodes and 256 active slave nodes on the ring.

There is no limit to the number of inactive nodes on a ring. There may be multiple inactive nodes with the same address numbers present on the ring.

Note that *stations* are devices that contain one or more MACRO nodes. *Nodes* that are contained within stations shall possess the actual master/slave address numbers.

Note

Normally, a system designer will require all nodes in a station to use the same master number, this choice is not a requirement of the MACRO standard. Using the same master number for all nodes in a station may simplify the process of binding (addressing) the nodes in a MACRO ring. In binding the ring addresses, master stations may possess active master nodes with the same master number, as long as they do not share the same slave number as well. Therefore it is possible for a MACRO ring to have 256 separate master stations, each with one active master node, even though there are only 16 master numbers.

When establishing the binding plan for a MACRO ring, there is no limitation regarding the ordering of stations on the ring. Physical order does not have to match any numerical order of node numbers, and master and slave stations may be mixed at will.

3.0 Physical Hardware Specifications

3.1 Network Hardware

3.1.1 Fiber Optic Protocol

3.1.1.1 Transmitter and Receiver Pair

Standard FDDI (Fiber Distributed Data Interface) optical transceiver pairs, compliant with the FDDI Physical Layer Medium Dependent (PMD) standard, ISO/IEC 9314-3, and ANSI X3.166-1990 shall be used.

The optical wavelength is 1300 nanometers.

The station-to-station distance with glass fiber shall be 3000 meters (~2 miles) capability minimum.

The recommended connector is SC-style, however, if the above physical specifications are maintained, other connector styles are acceptable. When other connector styles are used, adapters shall be available to achieve SC-style interconnections.

Note

An example of optical transceiver components that can be used include Hewlett-Packard's HFBR-5103 transceiver, and AMP's 269040-1 SC Duplex Transceiver.

3.1.1.2 Fiber Optic Cable

The recommended cable is a multi-mode glass fiber that has a multi-strand diameter of 62.5 micron. Glass multi-mode fiber cable shall be compliant with the FDDI Physical Layer Medium Dependent (PMD) standard, ISO/IEC 9314-3, and ANSI X3.166-1990.

When other fiber cable types are used, adapters shall be available to achieve connections per 3.1.1.1 above.

The station-to-station distance with glass multi-mode fiber shall be 3000 m (~2 miles) capability minimum. If other fiber cable types are used, the station-to-station distance performance may be reduced.

Note

A typical specification for glass fiber cable is 62.5/125 multi-mode. Underwriter's Laboratory has UL1666 rating OFNR. CSA specification is OFN FT4.

3.1.2 Wire Twisted Pair Protocol

3.1.2.1 Transmitter And Receiver Pair

The electrical signals are differential, 100K ECL-compatible, referenced (shifted) to operate from a +5V supply. They are NRZI PECL binary and may be active driven or transformer isolated.

Line impedance of twisted pair shielded or unshielded wire is 100Ω to 150Ω.

The recommended connector is RJ45 (8 pin) style, however, if the above physical specifications are maintained, other connector styles are acceptable. When other connector styles are used, adapters shall be available to achieve RJ45-style interconnections.

Typically, MACRO supports 8 pin RJ-45 "phone cord" non-flopped twisted-pair cables for interface between stations. The station-to-station distance capability with twisted pair cable shall exceed 3m (10 ft).

Note

This interface can be useful for compact but constrained wiring environments, such as the inside of robot arms.

3.2 Station Hardware

A single station may contain one or more nodes. These nodes contain master/slave addresses.

There may be more than one station contained in a single hardware device. Multiple stations contribute to multiple station delays when calculating MACRO ring loading.

4.0 Layer Structures For MACRO

4.1 Physical Layer

4.1.1 Serial I/O Transmission

4.1.1.1 Transmission Rate

MACRO data transmission shall be 125 megabit-per-second ±0.1% serial data stream.

A station shall be capable of handling a ±0.1% tolerance in data rate for the data that it receives, and shall not impose a greater than ±0.1% tolerance in the rate of the data that it transmits.

Note

The specifications for signal characteristics listed in this section are met automatically through use of Advanced Micro Devices TAXIchip™ set or equivalent running from a 12.5 MHz crystal.

4.1.2 Serial I/O Data

4.1.2.1 Serial Data Coding

Data shall be coded with both NRZI (non-return to zero, invert on ones) and 4B/5B coding.

NRZI represents a "1" by a transition and a "0" by the lack of transition.

4B/5B coding is used per ANSI X3T9.5 (FDDI).

With both NRZI and 4B/5B coding schemes used, there will always be at least 2 voltage transitions per symbol sent and never more than 3 consecutive non-transition bit times in any 10 bit pattern.

4.1.2.2 Command Bytes

Command bytes shall be used to indicate presence of MACRO ring (CMD-0), the start of a packet of data (Packet Header = CMD-1), and passing of the baton (CMD-1 + CMD-1).

When data is not being transmitted through the MACRO ring, CMD-0 shall be transmitted to maintain ring activity. A MACRO ring is not permitted to stand idle (no activity) between packet transmissions.

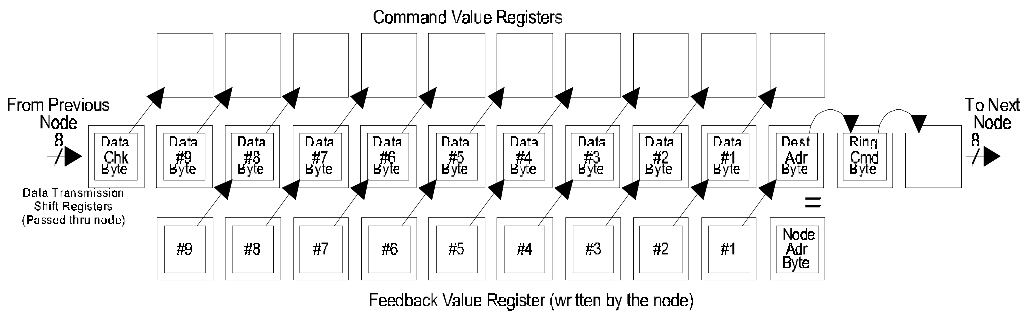
Data packets shall start with CMD-1.

A master passes its control to the next master by transmitting two CMD-1 words.

4.1.3 Data Packet Format

During a ring communication cycle, each active master node transmits one command (output) data packet to the ring, and receives one feedback (input) data packet from the ring in return.

The data packets that are sent from the master station into a ring shall be sent in multiples of 12 bytes. The first byte is a ring command byte followed by the destination address byte. The next 9 bytes contain the data that is being transmitted through the packet. The last byte is a checksum byte.



A MACRO station may have more than one active node, and therefore may send or receive multiple data packets during each ring communication cycle.

4.1.3.1 Command Byte

The first byte in the MACRO packet is the CMD-1 “command byte” which announces to any station on the ring that a packet of data is following.

This is the start of transmission word which tells the devices on the ring that the next data will be address data.

4.1.3.2 Address Byte

The second byte is the address byte. The address byte is typically organized as two 4-bit nibbles.

The most significant nibble carries the number of the master (0-15) from which the command packet originates, or to which a feedback packet is headed. The least significant nibble carries the number of the slave node (0-15) which is the destination of the packet.

	MASTER				SLAVE			
BIT #	7			4	3			0
	X	X	X	X	X	X	X	X

4.1.3.3 Data Bytes

The 3rd through 11th bytes contain the data fields of the packet, in either one of the standard application layer formats or a custom format as prescribed by the MACRO product's manufacturer.

4.1.3.4 Checksum Byte

The 12th byte is a checksum byte. Each bit in the byte corresponds to the even parity of the data that is in the destination address byte through the last data byte.

This process is performed by taking the exclusive-OR value of each byte from the destination address byte through the last data byte.

4.2 Logical Layers

MACRO uses two types of logical layer. These are called TYPE 0 and TYPE 1 protocols.

The difference between these two types of protocol comes from the desire to transmit either more nodes per ring (type 0) or more data per packet (type 1).

Type 0 has 16 nodes of data per master at 48 bits of data per node. This allows up to 16 master addresses with 16 slave addresses, 256 nodes per MACRO ring to be used. Master to slave communication is performed using MACRO reads and writes which allows the user to write up to 256 mailbox addresses from the master to the slave. The slave's status is monitored using a status word that is passed in the 24 bit register while it is not performing mailbox reads or writes. There is no master to master communication in type 0 MACRO.

Type 1 has 14 nodes of data per master at 72 bits of data per node. This allows ring addressing with 16 master addresses of 14 slave addresses per master. This allows 224 nodes per MACRO ring to be used. Master to slave communication is performed by addressing the slave device using node 15 while master to master communication is performed by addressing the master devices using node 14.

The nine bytes of data in each packet have a specific structure in the MACRO standard, detailed below.

4.2.1 Type 0 Register Structure

Each packet of data for a node contains 4 registers: 0, 1, 2, and 3. Register 0 is a 24-bit (3-byte) auxiliary register for non-real-time data. Registers 1, 2, and 3 are 16-bit (2-byte) registers for real-time data. Each node has a command packet of 4 registers and a feedback packet of 4 registers.

Register #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Master Command	Real-Time Register 3	Real-Time Register 2	Real-Time Register 1	Auxiliary Register Aux. Data | Ident.
Slave Feedback	Real-Time Register 3	Real-Time Register 2	Real-Time Register 1	Auxiliary Register Aux. Data | Ident.
Bit #	71··············56	55··············40	39··············24	23······················0

Real-Time registers are used to transmit and receive data in a parallel format. Each cycle of the ring carries data from the master to the slave station's MACRO registers while the slave station carries data back to the master station's registers.

Auxiliary registers are used to transmit and receive data that is not necessary for immediate transactions by the MACRO station. This information is sent as bit wide flags that may either command a MACRO station to perform an action or send its status back to the master station.

4.2.1.1 Auxiliary Register (type 0) Operation

There are 3 types of function that the auxiliary register performs in the type 0 MACRO ring.

The least significant 8 bits of the auxiliary register are used to establish a communication type between the master and slave device. The other 16 bits are used for passing parameters such as station status or register content.

Status information is exchanged with the MACRO station when the master is not commanding a register-based operation. This information is transmitted in a parallel bit-format while the master is in an idle state (no MACRO read or write is occuring). There is a pre-assigned set of bits established which shall be supported by all type 0 MACRO station devices.

MACRO Auxiliary Register Communication occurs when there is a need to deposit data or retrieve data from registers located in the MACRO station.

When a MACRO Master Execute Command is performed to a dedicated register address, an immediate station action is triggered.

4.2.1.1.1 Auxiliary Register Idle State (Status mode)

Status Mode

Master Command	Bits represent a command state to station	ID Code Idle state Data = 255
Slave Response	Bits represent the status of the station	ID Code Idle state Data = 00
Bit #	23 8	7 0

When the master sends an idle state word in the ID Code place (least significant 8 bits of the auxiliary register), the slave station shall respond by sending an idle state word as its ID Code (8 LSB bits).

While the master is transmitting the idle ID code, the other 16 bits of the auxiliary register shall contain bit flag data that tells the slave station something about how it should be operating.

While the slave station is receiving the idle ID code, the other 16 bits of the returned auxiliary register shall contain bit flag data that tells the master station something about the slave station's operating status.

Some of the bits are reserved for specific operating conditions and shall be specified as follows:

Master Idle State Auxiliary Register
Command Bits (Sent to slave)

Bit #		Description
00 - 07	—	Mode word 255 = Master Idle State
08	—	
09	—	
10	—	
11	—	Trigger Latch Enable
12	—	Node position reset command 1 = Reset
13	—	
14	—	Amp/Data Enable 1 = Enable
15	—	
16	—	
17	—	
18	—	
19	—	
20	—	
21	—	
22	—	
23	—	

Mode Word: The value in this 8 bit register (bit 00 - 07) implies that the node shall be either an idle state (this is when the other status bits are available) or a command state.

A command state is Master Read request, Master Write request, or Master Execute Command (Described in the next sections).

Trigger Latch Enable/
Trigger Latch: When bit #11 is set in the master, the slave node shall clear bit #11 (Bit #11=0).

This function shall allow a slave station to latch the status of an event that may represent a condition that occurs faster than the MACRO ring interface will allow.

NOTE

Slave Idle State Auxiliary Register
Status Bits (Returned to master)

Bit #		Description
00 - 07	—	Mode word 00 = Slave Idle State
08	—	
09	—	
10	—	
11	—	Trigger Latch
12	—	Power On Reset or Node reset has occurred 1 = Reset
13	—	MACRO Ring Break 1 = Ring communication failure
14	—	Amp/Data Enabled 1 = Amp/Data is Enabled
15	—	Station Node Fault (Amp Fault)
16	—	* Home flag Status
17	—	* Positive End Limit
18	—	* Negative End Limit
19	—	* User N Flag
20	—	* User W Flag
21	—	* User V Flag
22	—	* User U Flag
23	—	* User T Flag

Typical applications for the trigger latch include a higher speed home search for a motor or a change of data on an I/O device that has momentary switch inputs.

Node Position Reset/POR: When bit #12 is set in the master, the slave node shall be commanded to perform a variable reset. This may be used by systems that have counter registers in the slave nodes or variables that need to be reset occasionally.

The slave shall use this bit to indicate that a power-on-reset has occurred. A transition from 0 to 1 on bit #14 by the master shall reset this slave output.

MACRO Ring Break: This bit is only used by a slave station. Bit #13 shall be set in the slave node when the MACRO ring is no longer detected.

This occurs as the result of constantly receiving data errors (Receiver over/underrun, data incorrect parity, or data missing).

The slave station shall become a synchronizing master temporarily and shall transmit this bit until it perceives the errors to go away. When errors go away, the station shall reestablish the normal ring connection it had previously.

NOTE

It follows that the processes that are performed by the slave node that reestablishes its connection may be affected by a ring break error. Those processes are not required to be restarted when the ring is connected again. Only MACRO communication processes are expected to return to their previous state.

Amp/Data Enable: When bit #14 is set in the master, the slave node shall be commanded to enable its motor's amplifier or allow I/O to occur.

When the slave has an amp or I/O that is enabled, the slave shall set bit 14 to "1".

Station Node Fault: Bit #15 shall be set in the slave as an indication that there is a problem with the slave's component interface. For motor interfaces, this bit is returned as an amplifier fault.

This bit is not specified for operation by the master.

The bits that are marked with an asterisk are designed specifically for motion based interfaces. These bits may be specified for different purposes when the slave node is not used for a motion interface.

Home Flag: Bit #16 shall be set in the feedback status word for the status of a home flag input.

This bit is specified for operation by the slave node. The master node has no function assigned to this bit.

Positive & Negative End Limit Flags: Bits #17 & #18 shall be set in the feedback status word for the status of the positive and negative end limit flag inputs (if they exist at the node).

Bit #17 shall be the positive end limit, bit #18 shall be the negative end limit.

This bit is specified for operation by the slave node. The master node has no function assigned to this bit.

User Flag Inputs: Bits #19 through #23 shall be set in the feedback status word for the status of five flag inputs.

NOTE

When a motor is commutated by a controller there are usually 3 flags that are used to indicate its position before applying power to the motor. These flags are typically labeled T, U, V inputs and are referred to as hall effect inputs.

The other 2 flags, W, N, are spare inputs that may be specified for special applications.

These bits are specified for operation by the slave node. The master node has no function assigned to this bit.

4.2.1.1.2 Master Read Request

There are 4 steps involved in performing a master read request. The master shall send the ID code for a read request (01). The slave shall respond with an ACK code (255) or a NACK code (254). The master shall then send its idle ID code followed by the slave sending its idle ID code.

This 4 step process allows a slave station time to respond to the read request made by the master. It is allowed to take multiple ring cycles to complete a master read or write request.

The maximum number of ring cycles allowed for a slave station to return ACK or NACK shall not exceed 2048.

Step #1 - #2

MASTER Request

Reg Addr	ID Code
0 - 65535	1

⇒

SLAVE Response

Parameter	ID Code	
Reg Value	255	(ACK)
ERR Val	254	(NACK)

Step #3 - #4

MASTER Request

CMD bits	ID Code
xxxx	1

⇒

SLAVE Response

Status bits	ID Code	
Xxxx	0	ACK of idle

The number of registers available to read by the master is 65536. This value shall be based upon the size of available data in the 16 bit register address field (shown in step #1 above).

The slave response shall be ACK (255) to acknowledge receipt of the master request or NACK (254) to acknowledge that the request is from a non-accessible register as shown in step #2.

If the slave responds with an ACK, then the value contained in the parameter field shall be the data from the selected register.

If the slave responds with a NACK, then the value contained in the parameter field shall be an error code number.

4.2.1.1.3 Master Write Request

There are 4 steps involved in performing a master write request. The master shall send the ID code for register's value to write the register. The slave shall respond with an ACK code (255) or a NACK code (254). The master shall then send its idle ID code followed by the slave sending its idle ID code.

This 4 step process allows a slave station time to respond to the write request made by the master. It is allowed to take multiple ring cycles to complete a master read or write request.

The maximum number of ring cycles allowed for a slave station to return ACK or NACK shall not exceed 2048.

Step #1 - #2

MASTER Request

Reg Data	Reg Addr
16 bits	2 - 252

⇒

SLAVE Response

Parameter	ID Code	
Not Used	255	(ACK)
ERR Val	254	(NACK)

Step #3 - #4

MASTER Request

CMD bits	ID Code
Xxxx	255

⇒

SLAVE Response

Status bits	ID Code	
xxxx	0	ACK of idle

The number of registers available to write by the master shall be 250. This value shall be based upon the concept that the ID Codes are also used for Master Read Request (01), Master Execute Command Request (253), and Master Idle (255).

The range of addresses that shall be accessed by a Master Write Request is 2 - 252.

The slave response shall be ACK (255) to acknowledge receipt of the master request or NACK (254) to acknowledge that the request is from a non-accessible register as shown in step #2.

If the slave responds with an ACK, then the value contained in the parameter field shall not be used.

If the slave responds with a NACK, then the value contained in the parameter field shall be an error code number.

4.2.1.1.4 Master Execute Command Request

The Master Execute Command Request is identical in function to the Master Write Request to register #253. Upon receipt of data that is written to register #253, the MACRO station shall perform an immediate action.

Typical applications for this function are system reset and save parameters to EEROM memory.

4.2.1.2 Application Layer (type 0)

The application layer shall be defined as follows. When a node is described as an application that fits in the type 0 description, and it is not included as a pre-defined type here, it shall be defined as an I/O device type.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Torque Drive	Master Command	Torque Cmd.			Auxiliary Register
	Slave Feedback		Position Feedback		Auxilary Register

Torque Cmd: 16 bit signed value of torque to be applied at motor drive.

Position Feedback: 16 bit value of encoder position.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Velocity Drive	Master Command	Velocity Cmd.			Auxiliary Register
	Slave Feedback		Position Feedback		Auxiliary Register

Velocity Cmd: 16 bit signed value of velocity to be applied at motor drive.

Position Feedback: 16 bit value of encoder position.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Direct PWM	Master Command	Phase A Voltage Cmd	Phase B Voltage Cmd	Phase C Voltage Cmd	Auxiliary Register
Drive	Slave Feedback	Phase A Current	Phase B Current	Position	Auxiliary Register

Phase A, B, C Voltage Cmd: 16 bit signed value of voltage be applied to the 3 phases of the motor drive.

Phase A, B, Current Feedback: 16 bit signed value of current that is returned from the 2 phases of the motor drive. The third phase current is related to the difference of the two phases.

Position Feedback: 16 bit value of encoder position.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Phase Current	Master Command	Phase A Current Cmd.	Phase B Current Cmd.		Auxiliary Register
Drive	Slave Feedback		Position Feedback		Auxiliary Register

Phase A, B Current Cmd: 16 bit signed value of current to be applied to the 2 phases of the motor drive.

Position Feedback: 16 bit value of encoder position.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Position Drive	Master Command	Position Command			Auxiliary Register
	Slave Feedback	Position Feedback			Auxiliary Register

Position Command: 32 bit value of commanded position.

Position Feedback: 32 bit value of encoder position.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
I/O Devices	Master Command	Bits 47-32	Bits 31-16	Bits 15-0	Auxilary Register
	Slave Feedback	Bits 47-32	Bits 31-16	Bits 15-0	Auxilary Register

4.2.2 Type 1 Register Structure

Each packet of data for a node shall contain 4 real-time data registers: 0, 1, 2, and 3. Register 0 shall be a 24-bit (3-byte) register. Registers 1, 2, and 3 shall be 16-bit (2-byte) registers. Each node shall have a command packet of 4 registers and a feedback packet of 4 registers.

Register #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Master Command	Real-Time Register 3	Real-Time Register 2	Real-Time Register 1	Real-Time Register 0
Slave Feedback	Real-Time Register 3	Real-Time Register 2	Real-Time Register 1	Real-Time Register 0
Bit #	71··············56	55··············40	39··············24	23·······················0

Real-Time registers shall be used to transmit and receive data in a parallel format. Each cycle of the ring carries data from the master to the slave station's MACRO registers while the slave station carries data back to the master station's registers.

Every real-time register shall be written/read once during each ring cycle.

Nodes 14 and 15 shall be used to transmit data that is not necessary for immediate transactions by the MACRO station. This information shall be sent as a serial transaction between a master and a slave, or a master and another master which may command a station to perform an action or return register data.

Node 14 shall be used for master to master communication. Node 15 shall be used for master to slave communication. Both nodes 14 and 15 are not available for real-time data in type 1 MACRO ring implementations.

Note

Some master controllers may disable the operation of master to master communication. When this is done, node 14 may be used for real-time data transfers.

4.2.2.1 Node 15 - Master to Slave Communication (type 1 MACRO)

Master-to-Slave Communication shall occur as a way to pass parameters into registers on a MACRO station. The slave may receive up to 48 bits of data from its master and respond with up to 48 bits.

A slave shall not initiate Master-to-slave communication.

The 24 bit register of node 15 shall be used as the application header for the master to slave communication interface.

Three 16 bit registers shall be used to transmit and return data between the master and slave device. The data is represented as 48 bits which are written into a destination register. When the destination register is smaller than 48 bits, the most significant bits are ignored.

The maximum number of ring cycles allowed for a slave station to respond to a master to slave communication command shall not exceed 2048.

Type 1 Master-Slave Command Protocol

24 Bit AUX Register	Bit #	23 ···· 20	19	18	17	16	15 ···· 4	3 ···· 0
		Node Number	Cmd Msg	Spare	CMD Handshake	Write/ Read	Type Number	Data Type

1st Register (16 bit)	Bit #	15 ······ 00
		Data

2nd Register (16 bit)	Bit #	15 ······ 00
		Data

3rd Register (16 bit)	Bit #	15 ······ 00
		Data

Type 1 Master-Slave Feedback Protocol

24 Bit AUX Register	Bit #	23 ···· 20	19	18	17	16	15 ···· 4	3 ···· 0
		Node Number	Status Msg	Error	Status Handshake	Write/ Read	Type Number	Data Type

1st Register (16 bit)	Bit #	15 ······ 00
		Data

2nd Register (16 bit)	Bit #	15 ······ 00
		Data

3rd Register (16 bit)	Bit #	15 ······ 00
		Data

4.2.2.1.1 Auxiliary Register Application Header Description

The bits used for the application header (located in the 24 bit auxiliary register) in master to slave communication shall be specified as follows:

Node Number: This 4 bit field shall indicate which node the master to slave communication is occurring with.

The data that is sent by the master shall have the target slave node selected by these bits.

The target slave shall return the same value as the master in the Node Number field.

CMD/Status MSG: This field shall contain a single bit that indicates that the originator of the communication is a master.

The master shall set this bit to 1 to indicate that this is a command message. The slave shall set this bit to "0" to indicate that this is a slave feedback message.

Error/Spare: This 1 bit field shall be used only by the slave as a feedback error status register.

This feedback bit shall be "1" when the slave is returning an error code. When there is no error, this bit shall be "0".

The following error codes shall be dedicated for master to slave communication. Other codes may be returned if a slave station requires additional error interface values.

These codes shall be returned in the 1st Register as a 16 bit value if an error occurs.

Error Codes:

1 - ILLEGAL DATA TYPE
Not a recognized data type

2 - ILLEGAL DATA RANGE
This may occur as a result of a request that is out of range.

4 - COMMUNICATION TIME-OUT
Normally this value is user selected. This value may never exceed 2048 ring cycles.

5 - DUPLICATE SLAVE STATION ERROR
This occurs when the slave station receives bit #19 as "0".

CMD/Status Handshake: This 1 bit field shall be used by the master and slave as the method of starting the master to slave command exchange.

When the data in the master CMD Handshake bit is different from the data in the slave Status Handshake bit, a master to slave command exchange is occurring.

The slave shall change the Status Handshake to be the same as the CMD Handshake when it returns data back to the master. This indicates the end of the master to slave command and indicates that node 15 is in an idle state.

Write/Read: This 1 bit field is shall be used by the master to indicate whether the selected operation is a register write (bit #16 = "1") or a register read (bit #16 = "0").

The target slave shall return the same value as the master in the Write/Read field.

Data Type: There are 16 possible data types.
Currently defined are:
I-var = 0
CMD= 4

The I-var data type shall refer to a register that may be read/written to as a value from master to slave.

The CMD data type shall refer to an immediate command that is executed in the slave.

The value of the type number (explained below) shall determine which I-var or CMD to access.

Type Number: This is the number of the register or CMD to access. If the "data type" is an I-var, the value of type number shall be the register variable to access in the slave by the master. If the "data type" is a CMD, the value of type number shall be an immediate command to execute.

Currently defined CMD values are:

Type Number	Description of Command
0	Broadcast station address release
1	Clear all station faults
2	Reset station: Restore saved variables (If EErom)
3	Reset station: Use default variables
4	Save variables to EEROM (If implemented)

Type 1 Explanation of Master-to-Slave Read and Write Processes

The process used for reading and writing registers from master-to-slave is either a 2 or a 3-step process. This is outlined as follows:

1. Master Command: This shall be either a command to write, or a command to read. Immediate executable commands (commands that have a data type of CMD = 4) look like any other read or write command.

The master shall issue the command to a slave node by placing that node's address in bits 20 – 23 (Node Number) of the Auxiliary Register and toggling bit #17 (CMD/Status Handshake bit). As the command passes through the MACRO stations on the ring, each slave monitors node 15 for an address match.

2. Slave Response: There are 4 different actions that may occur in a station node as a result of the master-slave command being passed through the MACRO ring:

    A. Slave node not addressed by master-slave command, slave is passive at node 15.
    B. Slave node addressed by master-slave command, slave is active at node 15.
    C. Slave node not addressed by master-slave command, slave is active at node 15.
    D. Slave node addressed by master-slave command, slave is not active at node 15.

Not addressed by command, slave is not active at node 15-
When the master-slave command (step 1 above) passes into a slave node that does not have an address match, and it is a passive node (the node was not addressed by the master in the previous command). The command will pass through to the next node.

Addressed by command, slave is active at node 15-
When the slave node that the command is passing through is where the command is addressed, and it is an active node (this node was addressed by the master in the previous command). The slave shall place its response data into the appropriate 48 bits of real-time data registers, and match bit #17 to indicate that the slave node has responded. The response will be retrieved by the master in the next ring cycle.

Not addressed by command, slave is active at node 15-
When the slave node that the command is passing through is not where the command is addressed, but was accessed by the master in the previous command. The slave node shall shut off its node 15. The slave node then becomes a passive monitor of the activity on node 15 and proceeds to pass information through as a passive node. This process uses an extra ring cycle because the data was not retransmitted by the node when it was an active node.

Addressed by command, slave is active at node 15-

When the slave node that the command is passing through is where the command is addressed, but it is a passive node (this node was not addressed by the master in the previous command). The slave node shall turn on node 15, become active, and shall place its response data into the appropriate 48 bits of real-time data registers. The slave node shall match bit #17 to indicate that the slave node has responded. The response will be retrieved by the master in the next ring cycle.

Unlike Type 0 MACRO there is no idle response needed by either the master or the slave which uses up extra MACRO ring cycles during master-to-slave accesses. This allows the interface to operate more efficiently when a master is communicating with only 1 slave on the ring.

The master-to-slave command may take either two or three ring cycles. The master or the slave station may require more time to process commands depending upon the design of the station. Therefore, a master-to-slave command may actually take more ring cycles depending upon the hardware used.

4.2.2.2 Node 14 Ring Master-to-master Communication (type 1 MACRO)

Ring Master-to-master communication shall occur as a way to pass parameters into registers between the ring master station and other master stations. A target master may receive up to 48 bits of data from the ring master and respond with up to 48 bits.

The 24 bit register of node 14 shall be used as the application header for the ring master-to-master communication interface.

Three 16 bit registers shall be used to transmit and return data between the ring master and target master device. The data is represented as 48 bits which are written into a destination register. When the destination register is smaller than 48 bits, the most significant bits are ignored.

The maximum number of ring cycles allowed for a slave station to respond to a ring master-to-master communication command shall not exceed 2048.

Type 1 Ring Master-Master Command Protocol

	Bit #	23 ···· 20	19	18	17	16	15 ···· 4	3 ···· 0
24 Bit AUX Register		Master Number	Cmd Msg	Spare	CMD Handshake	Write/ Read	Type Number	Data Type

	Bit #	15 ··········· 00
1st Register (16 bit)		*Data*

	Bit #	15 ··········· 00
2nd Register (16 bit)		*Data*

	Bit #	15 ··········· 00
3rd Register (16 bit)		*Data*

Type 1 Master-to-Ring Master Feedback Protocol

	Bit #	23 ···· 20	19	18	17	16	15 ···· 4	3 ···· 0
24 Bit AUX Register		Master Number	Status Msg	Error	Status Handshake	Write/ Read	Type Number	Data Type

	Bit #	15 ··········· 00
1st Register (16 bit)		*Data*

	Bit #	15 ··········· 00
2nd Register (16 bit)		*Data*

	Bit #	15 ··········· 00
3rd Register (16 bit)		*Data*

4.2.2.2.1 Auxiliary Register Application Header Description

The bits in the application header for ring master-to-master communication are described as two different 24 bit words for the ring master and target master. They are actually the same word, but are described differently for clarification.

The bits used for the application header (located in the 24 bit auxiliary register) in master to master communication shall be specified as follows:

Master Number: This 4 bit field shall contain the address of the target master that communication is occurring with.

The target master station shall return the same value in the feedback Node Number field.

CMD/Status MSG: This field shall contain a single bit that indicates that the originator of the communication is a ring master.

The ring master shall set this bit to 1 to indicate that this is a command message. The target master shall set this bit to "0" to indicate that this is a master feedback message.

Error/Spare: This 1 bit field shall be used only by the target master as a feedback error status register.

This feedback bit shall be "1" when the target master is returning an error code. When there is no error, this bit shall be "0".

The following error codes shall be dedicated for ring master-to-master communication. Other codes may be returned if master stations require additional error interface values.

These codes shall be returned in the 1st Register as a 16 bit value if an error occurs.

Error Codes:

1 - ILLEGAL DATA TYPE
Not a recognized data type.

2 - ILLEGAL DATA RANGE
This may occur as a result of a request that is out of range.

4 - COMMUNICATION TIME-OUT
Normally this value is user selected. This value may never exceed 2048 ring cycles.

5 - DUPLICATE MASTER STATION ERROR
This occurs when the target master station receives bit #19 as "0".

CMD/Status Handshake: This 1 bit field shall be used by the ring master and target master as the method of starting ring master-to-master command exchange.

When the data in the source master CMD Handshake bit is different from the data in the target master Status Handshake bit, a master to slave command exchange is occurring.

The target master shall change the Status Handshake to be the same as the ring master's CMD Handshake when it returns data back to the source master. This shall indicate the end of the ring master-to-master command and indicates that node 15 is in an idle state.

Write/Read: This 1 bit field shall be used by the ring master to indicate whether the selected operation is a register write (bit #16 = "1") or a register read (bit #16 = "0").

The target master shall return the same value as the ring master in the Write/Read field.

Data Type: There are 8 possible data types.
Currently defined are:

I-var = 0
M-var=1
P-var=2
Q-var=3
CMD= 4
ASCII=5

Data types of 0 through 4 shall be used for register access. The I-var, M-var, P-var, Q-var data types imply a register paging scheme that may be read/written to as a value from the ring master to target master.

The CMD data type implies an immediate command that is executed in the target master.

The ASCII data type implies a sequential transmission of ASCII bytes that occurs 6 bytes at a time repeatedly until an ASCII NULL is transmitted.

The value of the type number (explained below) determines which I-var, M-var, P-var, Q-var, or CMD to access.

Type Number: This shall be the number of the register or CMD to access. If the "data type" is an I-var, M-var, P-var, Q-var the value of type number is the register variable to access in the slave by the master. If the "data type" is a CMD, the value of type number is the immediate command to execute.

Currently defined CMD values are:

Type Number	Description of Command
0	Broadcast (target master) station address release
1	Clear all station faults
2	Reset station: Restore saved variables (If EErom)
3	Reset station: Use default variables
4	Save variables to EEROM

4.2.2.3 Application Layer (type 1)

The application layer shall be defined as follows. When a node is described as an application that fits in the type 1 description, and it is not included as a pre-defined type here, it shall be defined as an I/O device type.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Torque Drive	Master Command	Motor Flag Command			Torque Cmd.
	Slave Feedback	Motor Flag Status			Position Feedback

Torque Cmd: 24 bit signed value of torque to be applied at motor drive.

Position Feedback: 24 bit value of encoder position.

When the data field value (such as Torque Cmd) is defined in the MACRO ring station hardware as less than the maximum bit field size (i.e. 24 bits), the data shall be left-shifted to the most significant bit position. This will allow hardware systems that do not match bit field sizes to maintain system-wide compatibility. The position feedback field shall be right-shifted.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Velocity Drive	Master Command	Motor Flag Command			Velocity Cmd.
	Slave Feedback	Motor Flag Status			Position Feedback

Velocity Cmd: 24 bit signed value of velocity to be applied at motor drive.

Position Feedback: 24 bit value of encoder position.

When the data field value (such as Velocity Cmd) is defined in the MACRO ring station hardware as less than the maximum bit field size (i.e. 24 bits), the data shall be left-shifted to the most significant bit position. This will allow hardware systems that do not match bit field sizes to maintain system-wide compatibility. The position feedback field shall be right-shifted.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Direct PWM	Master Command	Motor Flag Command	Phase C Voltage Cmd	Phase B Voltage Cmd	Phase A Voltage Cmd
Drive	Slave Feedback	Motor Flag Status	Phase B Current	Phase A Current	Position Feedback

Phase A Voltage Cmd: 24 bit signed value of voltage be applied to the 3 phases of the motor drive. The data should be placed left-shifted if less than 24 bits are used.

Phase B, C Voltage Cmd: 16 bit signed value of voltage be applied to the 3 phases of the motor drive.

Phase A, B, Current Feedback: 16 bit signed value of current that is returned from the 2 phases of the motor drive. The third phase current is related to the difference of the two phases.

Position Feedback: 24 bit value of encoder position.

When the data field value (such as Phase A Voltage Cmd) is defined in the MACRO ring station hardware as less than the maximum bit field size (i.e. 24 bits), the data shall be left-shifted to the most significant bit position. This will allow hardware systems that do not match bit field sizes to maintain system-wide compatibility. The position feedback field shall be right-shifted.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Phase Current	Master Command	Motor Flag Command		Phase B Current Cmd.	Phase A Current Cmd
Drive	Slave Feedback	Motor Flag Status			Position Feedback

Phase A Current Cmd: 24 bit signed value of current to be applied to the 2 phases of the motor drive.

Phase B Current Cmd: 16 bit signed value of current to be applied to the 2 phases of the motor drive.

Position Feedback: 24 bit value of encoder position.

When the data field value (such as Phase A Current Cmd) is defined in the MACRO ring station hardware as less than the maximum bit field size (i.e. 24 bits), the data shall be left-shifted to the most significant bit position. This will allow hardware systems that do not match bit field sizes to maintain system-wide compatibility. The position feedback field shall be right-shifted.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
Position Drive	Master Command	Motor Flag Command		Position Cmd 16 MSBs	Position Cmd 24 LSBs
	Slave Feedback	Motor Flag Status		Position Feedback 16 MSBs	Position Feedback 24 LSBs

Position Command 24 LSBs: 24 bit LSB value of commanded position.

Position Command 16 MSBs: 16 bit MSB value of commanded position.

Position Feedback 24 LSBs: 24 bit LSB value of encoder position.

Position Feedback 16 MSBs: 16 bit MSB value of encoder position.

The position command and position feedback fields shall be right-shifted for position drive protocol.

	Reg #	3 (16-bit)	2 (16-bit)	1 (16-bit)	0 (24-bit)
I/O Devices	Master Command	I/O Flag Command	Bits 47-32	Bits 31-16	Bits 15-0
	Slave Feedback	I/O Flag Status	Bits 47-32	Bits 31-16	Bits 15-0

5.0 Error Handling on the MACRO Ring

There are several levels of error detection built in to the MACRO communications protocol.

5.1 Serial Protocol Errors

Byte violation errors: Each byte shall be transmitted serially with two redundant bits (4B/5B protocol). If the receiving circuit detects errors in the data stream, a byte violation will occur.

The receiver circuit that converts the input bit stream back into an 8-bit parallel data stream shall also put out a "violation" bit telling whether it has received an error.

Each station shall look for violation errors on every byte it receives, even if these bytes are not part of a packet addressed to a node on the station.

When a violation error occurs as part of a packet addressed to a node on the station, active or inactive, the station shall not latch in the new data packet, which leaves the previous cycle's data in place. A slave station shall still substitute its feedback data packet for the erroneous command data packet.

If the violation error occurs as part of a packet not addressed to a node on the station, the station shall halt re-transmission of the data packet, even if the re-transmission has already started. The station containing the node to which the bad packet is addressed will reject it with a Packet Underflow Error, as described below.

Packet checksum errors: The last byte of the data packet is a checksum byte. Each bit shall be the odd parity bit for the corresponding bits of each previous byte in the packet.

If a checksum error occurs as part of a packet addressed to a node, active or inactive, the station shall not latch in the data packet. This leaves the previous cycle's data in place. A slave station shall still substitute its feedback data packet for the erroneous command data packet.

A station is not required to calculate the checksum for a packet not addressed to one of its nodes. When a packet is re-transmitted, whether received as an inactive node or not, the station shall re-transmit the checksum byte that it received.

Packet Underflow Errors: If there are less than 11 data bytes following a CMD-1 command byte before the next command byte is received, the station shall report a packet underflow error. The CMD-0 sync byte that the originating master sends after the data checksum byte in each packet is a command byte. This shall establish the packet length.

When an underflow error occurs as part of a packet addressed to a node on the station, active or inactive, the station shall not latch in the data packet, which leaves the previous cycle's data in place. A slave station should still substitute its feedback data packet for the erroneous command data packet.

Packet underflow errors can occur when an upstream station has detected a byte violation error in part of the packet, and stopped re-transmitting the rest of the packet.

Packet Overflow Errors: When there are more than 11 data bytes following a command byte before the next command byte is received, the station should report a packet overflow error.

If a packet overflow error occurs as part of a packet addressed to a node on the station, active or inactive, the station shall not latch in the data packet, which leaves the previous cycle's data in place. A slave station should still substitute its feedback data packet for the erroneous command data packet.

5.2 Ring Protocol Errors

Ring Break Detection: A MACRO station shall detect a ring break between it and the upstream station when it receives continuous byte violation errors.

Since ring break is characterized by continuous violation errors, it may be difficult to determine how many consecutive violation errors should be received before a station declares a ring break.

A *Ring Break Detection* shall occur when more than 5 ring cycles occur with violation errors. The *Ring Break Detection* shall be determined by a station in less than 2048 ring cycles.

When a station detects a ring break, it shall turn itself into a master and transmit the "ring break" bit in the status flag back to its master station. This will allow a master station to perform an action (i.e. illuminate a beacon light) to react to the ring break indication.

6.0 Calculating Ring Network Frequencies

MACRO networks are designed to communicate at a fixed frequency. The components used in the ring affect three factors relating to communications frequency.

These are:

1. The number of data packets sent per ring cycle (equals the number of active master nodes)
2. The number of stations on the ring, each with a transceiver delay
3. The length of the conductors between stations, allowing for the speed of light (fiber system) or electromagnetic radiation (copper system).

6.1 Number Of Data Packets Sent Per Ring Cycle

The fundamental transmission rate of a MACRO network is 125 megabits per second (Mbps). The protocol of each transmission occurs as 4B/5B (ANSI X3T9.5 FDDI) coded data. Each actual byte is transmitted as 10 bits, which includes 2 redundant bits, for a rate of 12.5 megabytes per second. Each data packet consists of 12 bytes, resulting in a rate just over 1 million packets per second. It takes just under 1 microsecond for a single packet to pass a given point on the ring.

6.2 Number Of Stations

A packet encounters a delay in passing through each station. This delay occurs because the data is de-serialized, then evaluated for an address match. If a match is made, then as the new data is shifted into the receiver registers, the transmitter registers shift data out onto the MACRO ring. If a match is not made, then the data is shifted directly back onto the MACRO ring. While the exact delay at a station is dependent on the design of the hardware in a station, typical delays are 0.5 to 0.6 microseconds per station.

6.3 Length Of Conductors

Data transmission is delayed by the speed of electromagnetic radiation in the fiber or copper conductors. This speed is about .004 µsec meter in fiber or copper.

Note

Unless the total conductor length in a MACRO ring is very long (i.e. 1 kilometer) this is not a significant factor in limiting the ring update rate and in most applications this parameter may be ignored.

The minimum time for a ring communications cycle can be calculated as:

Min_time = 1.0 µsec * (Number of active master nodes)
+ 0.6 µsec * (Number of stations)
+0.004 µsec * (total meters of conductors)

Example: A MACRO network has 36 active master nodes on 4 master stations. The matching slave nodes exist on 24 slave stations. The total cable length is 100 meters The minimum time for a ring communications cycle is:

Min_time = 1.0µsec * 36 + 0.6µsec * (4+24) + 0.004µsec * 100 = 53.4µsec

The MACRO ring frequency is then:

Max_frequency = 1 / 53.4µsec = 18.7 kHz

Note

When calculating the maximum frequency expected for a MACRO ring, the designer should be aware that this maximum value is not to be exceeded. Therefore, it is advisable to insure that there is an additional 10% added to the calculated ring time for practical design considerations.

APPENDIX

A1.0 ANSI X3T9.5 (FDDI) 4B/5B Coding

In using 4B/5B coding, each nibble of the byte is represented as a 5-bit quantity, with a redundant bit for error checking. The 10 bits representing the byte are shifted out with the most significant bit of the most significant nibble coming out first.

The 4B/5B code encodes a byte (8 bits) of data as two nibbles, each represented as 5 bits, by the following patterns:

Hex Data	4-bit value	5-bit pattern	Hex Data	4-bit value	5-bit pattern
0	0000	11110	8	1000	10010
1	0001	01001	9	1001	10011
2	0010	10100	A	1010	10110
3	0011	10101	B	1011	10111
4	0100	01010	C	1100	11010
5	0101	01011	D	1101	11011
6	0110	01110	E	1110	11100
7	0111	01111	F	1111	11101

A1.1 Command Byte Coding

Sixteen 10-bit patterns not used by data byte encoding in the 4B/5B code are reserved for “command bytes”, labeled CMD-0 through CMD-F (15).

CMD-0 is automatically transmitted when no other command or data byte is being sent. This is called the “sync byte”, because its purpose is to maintain synchronization between stations when no data is being sent and so a station knows the difference between a temporarily idle ring and a broken ring. The sync byte is represented by CMD-0 (11000 10001).

MACRO uses CMD-1 as a packet header, the first byte of the packet that notifies the receiving station that a data packet has arrived. It is represented by (11111 11111).

CMD-2 through CMD-F not used in the MACRO standard.

Note

The specifications of the byte formatting are met automatically through use of the Advanced Micro Devices TAXIchip^{TM} set or equivalent transmitter and receiver ICs.

A1.2 Baton Signal Format

The “baton signal” consists of two consecutive CMD-1 command bytes.

The baton signal is used to signal the next master in the MACRO ring to start transmitting data packets. Each master transmits the baton signal at the end of its transmissions, passing it downstream to the next master in the ring.