MACROGATE

Motion And Control Ring Optical Gate Array

Features

- Glue-less TAXIchip™ Interface
- 16 Nodes of 72-Bit Data Registers
- Internal 120 Mhz Phase Locked Loop
- 24-Bit Latchable Input Pins
- 24-Bit Programmable Output Pins
- A/B Quadrature Decoder with Digital Noise Filter
- 24-Bit Encoder Counter with Programmable Sample Clock
- Configurable for 24,16 or 8-Bit Processor Bus Interface

Applications

- Smart Motor Controller Interface
- I/O Device Driver Interface
- Digital Video Adapter Interface
- Digital Audio Adapter Inteface

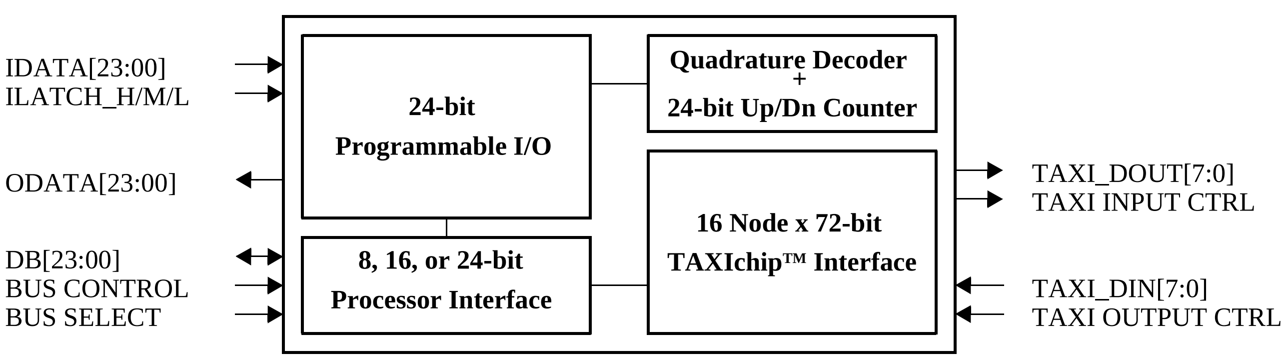
Description

The Delta Tau MACROGATE chip provides a glue-less interface to the AMD TAXIchip™ (Transparent Asynchronous Transmit/Receive Interface) chip set. With the MACROGATE, it is now easy to construct a fiber optic ring for high-speed data transfers without the burdens of multi-conductor cables, crosstalk, and Radio Frequency Interference (RFI).

The Delta Tau MACROGATE also contains a 24-bit programmable output port for setting control lines, switches, etc. Complementing the output port is the 24-bit latchable input port readable through the processor interface. Three separate latch controls, with programmable polarity, allow for latching of individual bytes within the 24-bit word.

Also in the MACROGATE is an A/B quadrature decoder and up/down counter for an easy interface to a position encoder. To improve noise immunity, both inputs to the A/B quadrature decoder are passed through a simple, yet effective digital filter. The output of the quadrature decoder feeds a 24-bit encoder counter with up and down counting. The count is directly readable through the processor interface.

Simplified Block Diagram



Pin Description

Table 1: MACROGATE Pin Description

Pin #	Name	Type	Description
1	VDD	Power	Power Supply, +5 Volts.
2	TAXI_DIN0	Input, Schmitt	TAXI interface data in, bit 0.
3	TAXI_DIN1	Input, Schmitt	TAXI interface data in, bit 1.
4	TAXI_DIN2	Input, Schmitt	TAXI interface data in, bit 2.
5	TAXI_DIN3	Input, Schmitt	TAXI interface data in, bit 3.
6	TAXI_DIN4	Input, Schmitt	TAXI interface data in, bit 4.
7	TAXI_DIN5	Input, Schmitt	TAXI interface data in, bit 5.
8	TAXI_DIN6	Input, Schmitt	TAXI interface data in, bit 6.
9	TAXI_DIN7	Input, Schmitt	TAXI interface data in, bit 7.
10	TAXI_DSTROBE	Input, Schmitt	TAXI interface data strobe pin.
11	TAXI_CIN	Input, Schmitt	TAXI interface command bit in.
12	TAXI_CSTROBE	Input, Schmitt	TAXI interface command strobe pin.
13	TAXI_VLTN	Input, Schmitt	TAXI interface violation flag pin.
14	TAXI_TCLK	Input, Schmitt	TAXI interface TCLK.
15	TAXI_MODE	Input, Schmitt	TAXI interface mode select. When TAXI_MODE = 0, this selects the normal input mode: data is received from the TAXI interface. When TAXI_MODE = 1, this selects the MACRO-to-MACRO interface: data is received from another MACRO chip.
16	RESET_N	Input, Schmitt	Master chip reset. This pin is active low.
17	GND	Ground	Power Supply, Ground.
18	GND	Ground	Power Supply, Ground.
19	GND	Ground	Power Supply, Ground.
20	TAXI_DOUT0	Output, 4mA	TAXI interface data out, bit 0.
21	TAXI_DOUT1	Output, 4mA	TAXI interface data out, bit 1.
22	TAXI_DOUT2	Output, 4mA	TAXI interface data out, bit 2.
23	TAXI_DOUT3	Output, 4mA	TAXI interface data out, bit 3.
24	TAXI_DOUT4	Output, 4mA	TAXI interface data out, bit 4.
25	TAXI_DOUT5	Output, 4mA	TAXI interface data out, bit 5.
26	TAXI_DOUT6	Output, 4mA	TAXI interface data out, bit 6.
27	TAXI_DOUT7	Output, 4mA	TAXI interface data out, bit 7.
28	TAXI_COUT	Output, 4mA	TAXI inteface command bit out.
29	TAXI_STROBEOUT	Output, 4mA	TAXI inteface command strobe out.

Table 1: MACROGATE Pin Description

Pin #	Name	Type	Description
30	GND	Ground	Power Supply, Ground.
31	PLLCLK	Input	Phase-locked loop reference clock input. This clock is internally multiplied 6x by the on-chip PLL. The allowable frequency range is 15.667 to 20.000 Mhz. Typically, 19.6608 Mhz is used as the reference frequency.
32	PLL_EN_N	Input	Phase-locked loop enable. This pin must be grounded for the phase-locked loop to operate.
33	VCOIN	Input	Phase-locked loop VCO input. This is an analog input fed by the external loop filter. See PLL Section for loop filter configuration and RC values.
34	CPOUT	Output	Phase-locked loop charge pump output. This analog output feeds the external loop filter. See PLL Section for loop filter configuration and RC values.
35	PLLVSS	PLL Ground	Power Supply, Ground. Care must be exercised in PCB layout to minimize noise on this analog supply pin.
36	PLLVDD	PLL Power	Power Supply, +5 Volts. Care must be exercised in PCB layout to minimize noise on this analog supply pin.
37	VDD	Power	Power Supply, +5 Volts.
38	IDATA00	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 00. Latching of the input data is controlled by ILATCH_L.
39	IDATA01	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 01. Latching of the input data is controlled by ILATCH_L.
40	IDATA02	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 02. Latching of the input data is controlled by ILATCH_L.
41	IDATA03	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 03. Latching of the input data is controlled by ILATCH_L.
42	IDATA04	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 04. Latching of the input data is controlled by ILATCH_L.
43	IDATA05	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 05. Latching of the input data is controlled by ILATCH_L.
44	IDATA06	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 06. Latching of the input data is controlled by ILATCH_L.
45	IDATA07	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 07. Latching of the input data is controlled by ILATCH_L.
46	IDATA08	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 08. Latching of the input data is controlled by ILATCH_M.
47	IDATA09	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 09. Latching of the input data is controlled by ILATCH_M.
48	IDATA10	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 10. Latching of the input data is controlled by ILATCH_M.
49	IDATA11	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 11. Latching of the input data is controlled by ILATCH_M.

Table 1: MACROGATE Pin Description

Pin #	Name	Type	Description
50	IDATA12	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 12. Latching of the input data is controlled by ILATCH_M.
51	IDATA13	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 13. Latching of the input data is controlled by ILATCH_M.
52	IDATA14	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 14. Latching of the input data is controlled by ILATCH_M.
53	GND	Ground	Power Supply, Ground.
54	PHASE	Bi-direct[2],4mA	Phase clock input/output. The MACROGATE chip can be configured to accept an external Phase clock. This pin has an open-drain output, so an external pull-up resistor is required if this pin is to be used by another digital input.
55	GND	Ground	Power Supply, Ground.
56	IDATA15	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 15. Latching of the input data is controlled by ILATCH_M.
57	IDATA16	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 16. Latching of the input data is controlled by ILATCH_H.
58	IDATA17	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 17. Latching of the input data is controlled by ILATCH_H.
59	IDATA18	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 18. Latching of the input data is controlled by ILATCH_H.
60	IDATA19	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 19. Latching of the input data is controlled by ILATCH_H.
61	IDATA20	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 20. Latching of the input data is controlled by ILATCH_H.
62	IDATA21	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 21. Latching of the input data is controlled by ILATCH_H.
63	IDATA22	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 22. Latching of the input data is controlled by ILATCH_H. This pin also functions as the B input to the A/B quadrature decoder.
64	IDATA23	Input, Schmitt, Pull-Up[1]	Input latch data input, bit 23. Latching of the input data is controlled by ILATCH_H. This pin also functions as the A input to the A/B quadrature decoder.
65	ILATCH_H	Input, Schmitt	Input data latch control, high byte. The latch is transparent when ILATCH_H = 1. Latching occurs on the falling edge. The polarity of this pin can be inverted by setting ILATCH_INV = 1.
66	ILATCH_M	Input, Schmitt	Input data latch control, mid byte. The latch is transparent when ILATCH_M = 1. Latching occurs on the falling edge. The polarity of this pin can be inverted by setting ILATCH_INV = 1.
67	ILATCH_L	Input, Schmitt	Input data latch control, low byte. The latch is transparent when ILATCH_L = 1. Latching occurs on the falling edge. The polarity of this pin can be inverted by setting ILATCH_INV = 1.
68	ILATCH_INV	Input, Schmitt	Input latch control invert.

Table 1: MACROGATE Pin Description

Pin #	Name	Type	Description
69	RD_N	Input, Schmitt	Processor interface read strobe. This pin is active low.
70	WR_N	Input, Schmitt	Processor interface write strobe. This pin is active low.
71	CS_N	Input, Schmitt	Processor interface chip select. This pin is active low.
72	VDD	Power	Power Supply, +5 Volts.
73	VDD	Power	Power Supply, +5 Volts.
74	ADDR0	Input, Schmitt	Processor interface address bit 0.
75	ADDR1	Input, Schmitt	Processor interface address bit 1.
76	ADDR2	Input, Schmitt	Processor interface address bit 2.
77	ADDR3	Input, Schmitt	Processor interface address bit 3.
78	ADDR4	Input, Schmitt	Processor interface address bit 4.
79	ADDR5	Input, Schmitt	Processor interface address bit 5.
80	ADDR6	Input, Schmitt	Processor interface address bit 6.
81	DB00	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 00.
82	DB01	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 01.
83	DB02	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 02.
84	DB03	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 03.
85	DB04	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 04.
86	DB05	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 05.
87	DB06	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 06.
88	DB07	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 07.
89	DB08	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 08.
90	GND	Ground	Power Supply, Ground.
91	GND	Ground	Power Supply, Ground.
92	GND	Ground	Power Supply, Ground.
93	DB09	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 09.

Table 1: MACROGATE Pin Description

Pin #	Name	Type	Description
94	DB10	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 10.
95	DB11	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 11.
96	DB12	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 12.
97	DB13	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 13.
98	DB14	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 14.
99	DB15	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 15.
100	DB16	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 16.
101	DB17	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 17.
102	DB18	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 18.
103	DB19	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 19.
104	DB20	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 20.
105	DB21	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 21.
106	DB22	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 22.
107	DB23	Bi-direct[2], 4mA, Pull-Up[1]	Processor interface data bus bit 23.
108	VDD	Power	Power Supply, +5 Volts.
109	VDD	Power	Power Supply, +5 Volts.
110	SUB_ADDR0	Input, Schmitt, Pull-Up[1]	Processor interface sub-address bit 0. Sub-addressing is used with 16 and 8 bit buses only.
111	SUB_ADDR1	Input,Schmitt, Pull-Up[1]	Processor interface sub-address bit 1. Sub-addressing is used with 16 and 8 bit buses only.
112	BUS_SEL0	Input, Schmitt	Processor interface bus select, bit 0.
113	BUS_SEL1	Input, Schmitt	Processor interface bus select, bit 1.

Table 1: MACROGATE Pin Description

Pin #	Name	Type	Description
114	TEST	Input, Schmitt	Test mode select pin. Setting TEST = 1 will place the chip into test mode. For normal operation, this pin must be grounded.
115	TEST_CLK	Input, Schmitt	Test mode clock pin. For normal operation, this pin must be grounded.
116	TEST_OUT	Output, 4mA	Test mode output pin.
117	ODATA00	Output, 4mA	Output data port, bit 00.
118	ODATA01	Output, 4mA	Output data port, bit 01.
119	ODATA02	Output, 4mA	Output data port, bit 02.
120	ODATA03	Output, 4mA	Output data port, bit 03.
121	ODATA04	Output, 4mA	Output data port, bit 04.
122	GND	Ground	Power Supply, Ground.
123	VDD	Power	Power Supply, +5 Volts.
124	GND	Ground	Power Supply, Ground.
125	ODATA05	Output, 4mA	Output data port, bit 05.
126	ODATA06	Output, 4mA	Output data port, bit 06.
127	ODATA07	Output, 4mA	Output data port, bit 07.
128	ODATA08	Output, 4mA	Output data port, bit 08.
129	ODATA09	Output, 4mA	Output data port, bit 09.
130	ODATA10	Output, 4mA	Output data port, bit 10.
131	ODATA11	Output, 4mA	Output data port, bit 11.
132	ODATA12	Output, 4mA	Output data port, bit 12.
133	ODATA13	Output, 4mA	Output data port, bit 13.
134	ODATA14	Output, 4mA	Output data port, bit 14.
135	ODATA15	Output, 4mA	Output data port, bit 15.
136	ODATA16	Output, 4mA	Output data port, bit 16.
137	ODATA17	Output, 4mA	Output data port, bit 17.
138	ODATA18	Output, 4mA	Output data port, bit 18.
139	ODATA19	Output, 4mA	Output data port, bit 19.
140	ODATA20	Output, 4mA	Output data port, bit 20.
141	ODATA21	Output, 4mA	Output data port, bit 21.
142	ODATA22	Output, 4mA	Output data port, bit 22.
143	ODATA23	Output, 4mA	Output data port, bit 23.
144	VDD	Power	Power Supply, +5 Volts.

Notes: All Schmitt trigger inputs are at TTL levels.

1. Pull-up resistance is between 20kΩ and 250kΩ.
2. These bi-directional buffers have Schmitt trigger inputs.

Electrical Characteristics

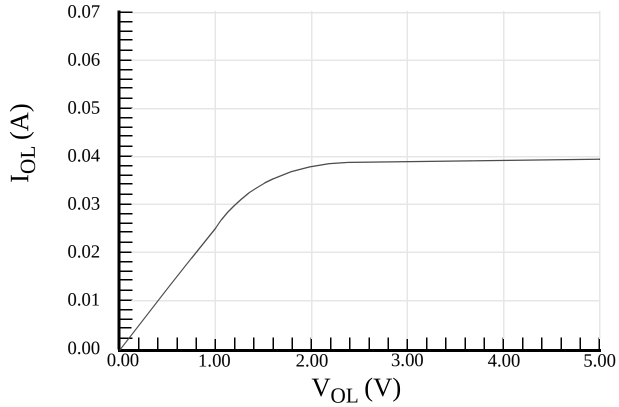
Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Supply Voltage	VDD	-0.6 - 7.0	V
Input Voltage	V_{IN}	-0.6 - VDD+0.6	V
DC Output Current	I_{OUT}	8 mA	mA
Storage Temperature	T_{STG}	-55 - 125	^oC

DC Characteristics

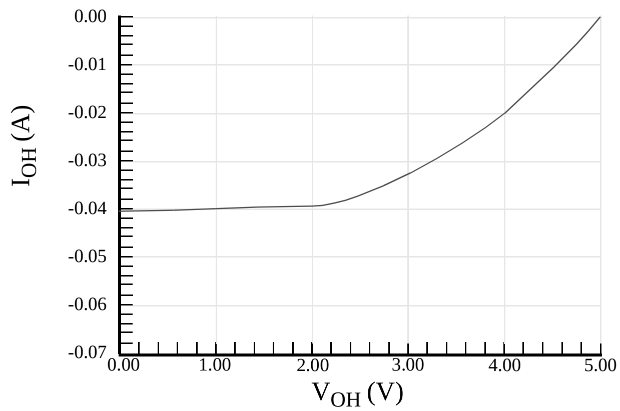
Symbol	Parameter	Condition	Limit MIN	Limit TYP	Limit MAX	Units
VDD	Supply voltage	-	4.50	5.00	5.50	V
V_{IH}	Input high voltage	TTL	2.0			V
V_{IL}	Input low voltage	TTL			0.8	V
V_+	Input high voltage	TTL Schmitt		1.66	2.15	V
V_-	Input high voltage	TTL Schmitt	0.60	1.13		V
V_H	Hysteresis voltage	TTL Schmitt	0.30			V
I_{IH}	Input high current	V_{IN} = VDD	-10		10	uA
I_{IL}	Input low current	V_{IN} = VSS	-10		10	uA
V_{OH}	Output high voltage	I_{OH} = -4 mA	3.5			V
V_{OL}	Output low voltage	I_{OH} = 4 mA			0.4	V
I_{OZ}	3-state leakage current	V_{OH} = VSS	-10		10	uA
I_{OZ}	3-state leakage current	V_{OL} = VDD	-10		10	uA
I_{PU}	Active pull-up current	V_{IN} = VSS	-20	-95	-250	uA

Output Current Capability



V_{OL} - I_{OL} Characteristics

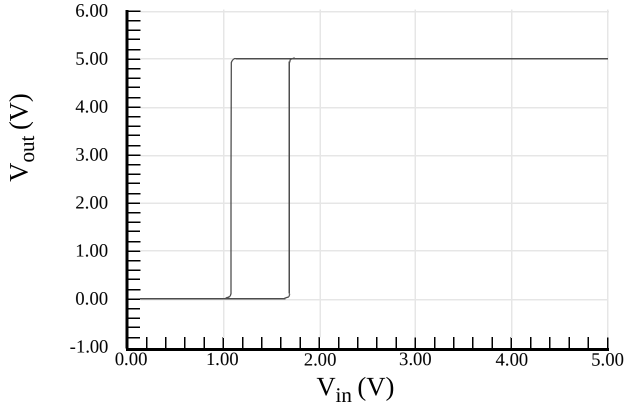
Figure 1: Output Buffer DC Characteristics



V_{OH} - I_{OH} Characteristics

Figure 2: Output Buffer DC Characteristics

Input Characteristics



V_{in} - V_{out} Characteristics (TTL Schmitt Trigger)

Figure 3: Input Buffer Switching Characteristics

Pinout

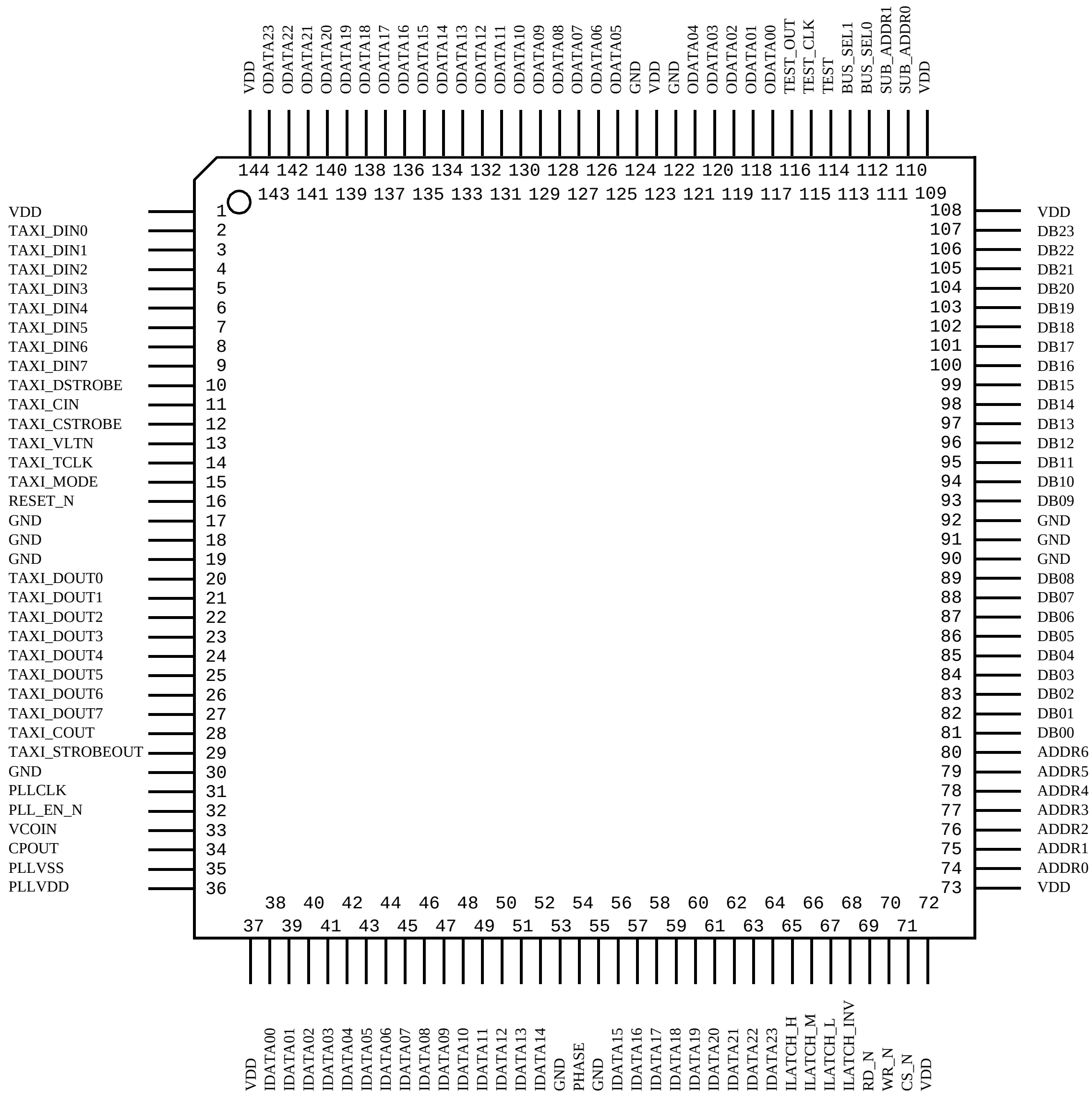


Figure 4: MACROGATE Chip Pinout

Phase-Locked Loop

The MACROGATE has an on-chip phase-locked loop (PLL) which is used to generate an internal clock six times the input reference clock frequency. For a reference clock of 20 Mhz, the internal clock used by the MACRO interface logic and the sample clock generator is 120 Mhz. The reference clock frequency may be between 15.667 Mhz and 20.000 Mhz, and is typically fixed at 19.6608 Mhz.

For reliable operation of the phase-locked loop, the analog power supply pins used by the PLL must be carefully routed on the PCB to minimize noise coupling. The PLL requires an external loop filter, shown in Figure 5, which must be placed close to the PLL pins to minimize noise. Table 2 lists the correct filter component values.

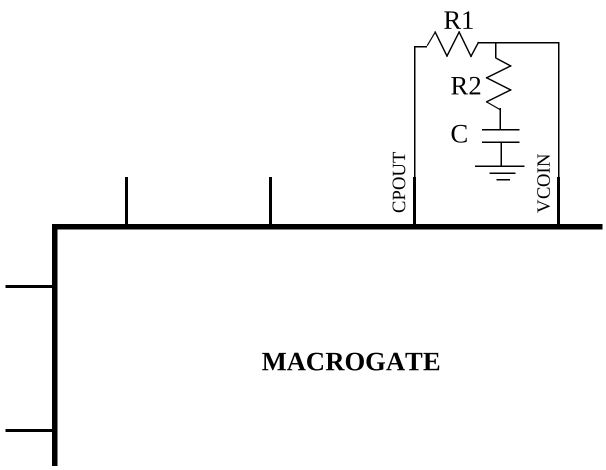


Figure 5: PLL Loop Filter

Table 2: PLL Loop Filter Component Values

Component	Value
R1	10 kΩ
R2	200 Ω
C	0.01 uF

Processor Interface

The MACROGATE chip has a pin configurable processor data bus interface. The user has the choice of selecting an 8-bit, 16-bit, or 24-bit data bus. The 16-bit bus has two separate options, giving the user the choice of byte alignment in reading 8-bit data. Table 3 describes the possible bus selections.

Internal to the MACROGATE, all data registers are 24 bits in width. Therefore, using the MACROGATE with 8 or 16-bit processors requires multiple read and write operations to access any of the 24-bit data registers. Accessing the individual bytes within the 24-bit data registers is done through the sub-address pins, SUB_ADDR[1:0]. Setting the sub-address to 00_B, selects the most significant 8 or 16 bits for an 8-bit or 16-bit interface, respectively. Setting the sub-address to 01_B, used only by the 8-bit interface, selects the middle significant 8 bits. And, setting the sub-address to 10_B, selects the least significant 8 or 16 bits for an 8-bit or 16-bit interface, respectively. For the 24-bit mode, the sub address pins are don't care.

For read operations, sub-addressing must be performed in the order described in Figures 6 through 9. The reason for this is that the read operation for sub-address 00_B latches the 24-bit data into a holding register, where subsequent reads of the remaining bits are protected against change in the main 24-bit register.

Likewise, for write operations, the sub-addressing must be performed as described in Figures 10 through 13. The reason for this is that the write operations for sub-addresses 01_B and 10_B are directed into a 24-bit buffer register. The final write operation for sub-address 00_B is what transfers the 24-bit data in the buffer register into the intended address location.

Table 3: Processor Bus Options

BUS_SEL1	BUS_SEL0	Data Bus	Description
0	0	DB[23:00]	24-Bit data bus interface.
0	1	DB[15:00]	16-Bit data bus interface, Mode A.
1	0	DB[15:00]	16-Bit data bus interface, Mode B.
1	1	DB[07:00]	8-Bit data bus interface.

Read Cycle Timing

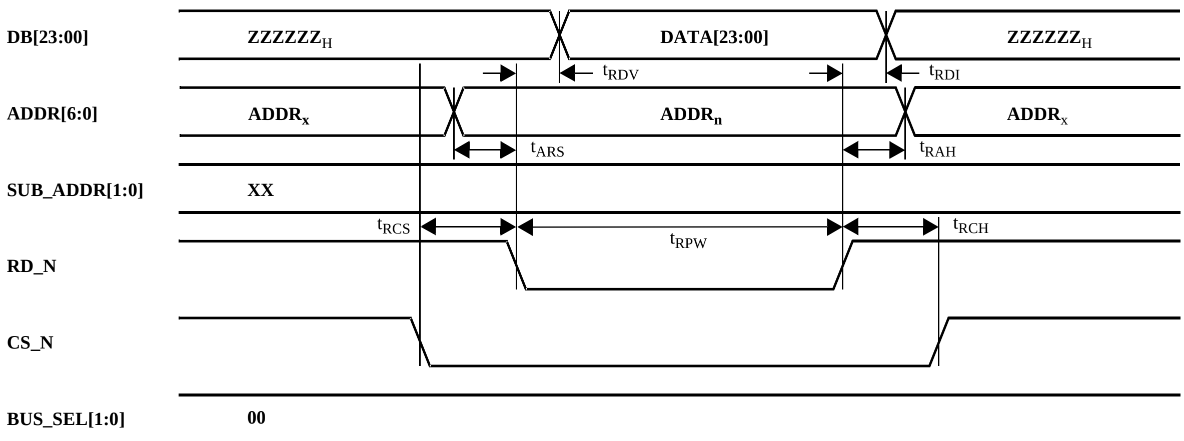


Figure 6: 24-Bit Data Bus Interface

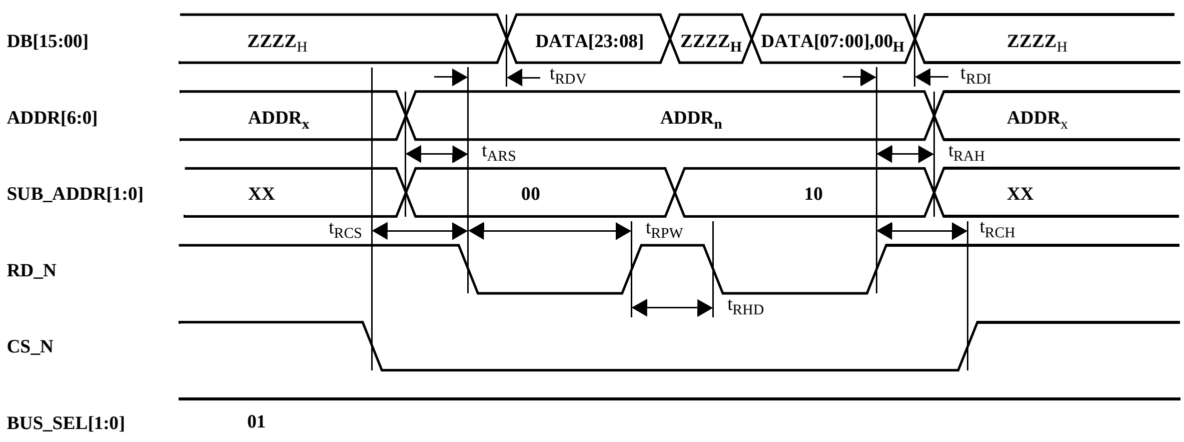


Figure 7: 16-Bit Data Bus Interface: Mode A

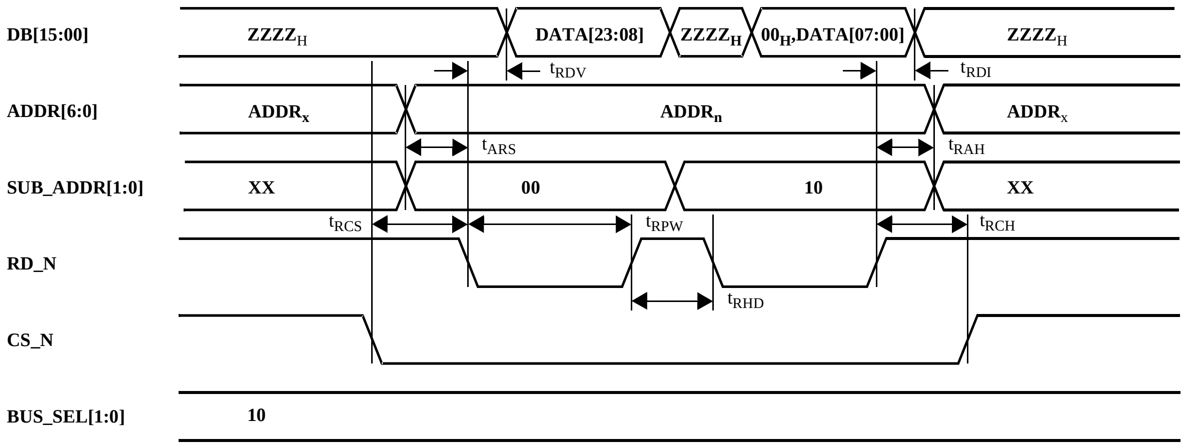


Figure 8: 16-Bit Data Bus Interface: Mode B

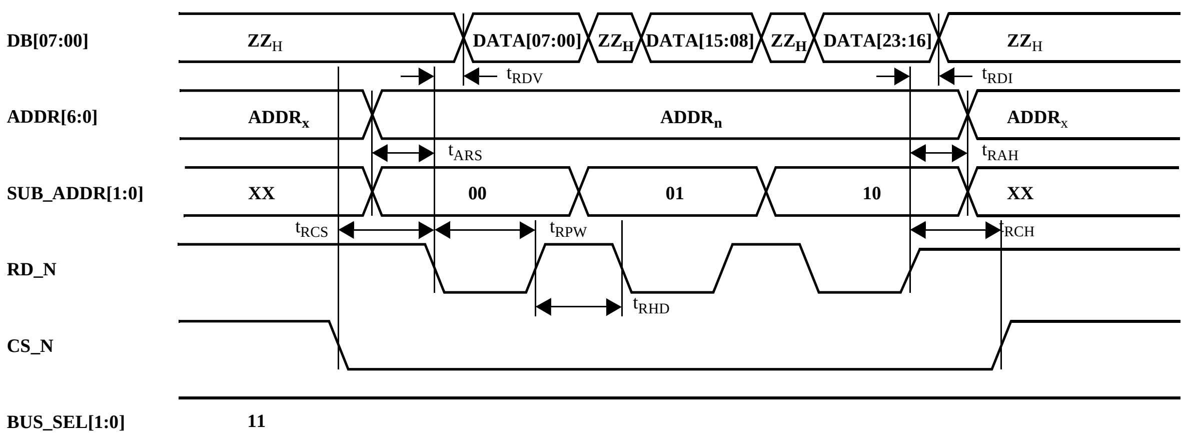


Figure 9: 8-Bit Data Bus Interface

Table 4: Read Cycle Timing Specifications V_{CC} = 5.0V $\pm$ 10%, T_A = 0^o to $+70^oC$, C_{LOAD} = 50 pF

Symbol	Parameter Description	Min	Max	Units
t_{RCS}	RD_N to CS_N Set Up	0		ns
t_{RCH}	RD_N to CS_N Hold	0		ns
t_{RPW}	RD_N Pulse Width	35		ns
t_{RHD}	RD_N High Delay	18		ns
t_{ARS}	ADDR to RD_N Set Up	0		ns
t_{RAH}	RD_N to ADDR Hold	0		ns

Table 4: Read Cycle Timing Specifications V_{CC} = 5.0V ± 10%, T_A = 0^o to $+70^oC$, C_{LOAD} = 50 pF

Symbol	Parameter Description	Min	Max	Units
t_{RDV}	RD_N to Data Valid		25	ns
t_{RDI}	RD_N to Data Invalid	3		ns

Write Cycle Timing

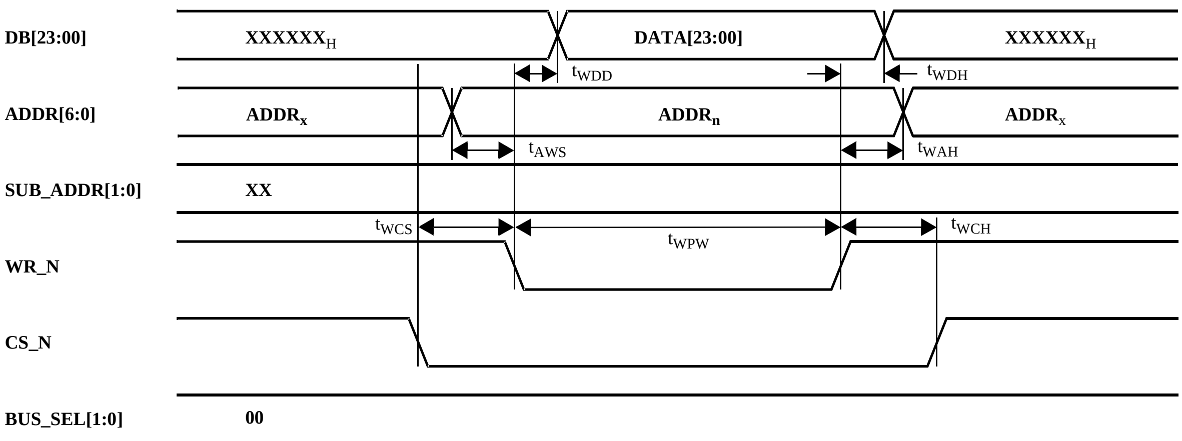


Figure 10: 24-Bit Data Bus Interface

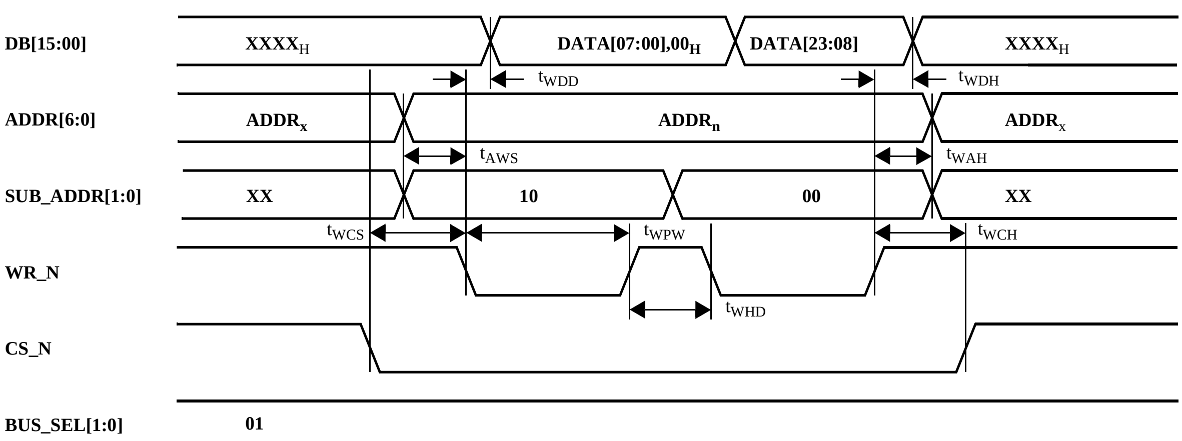


Figure 11: 16-Bit Data Bus Interface: Mode A

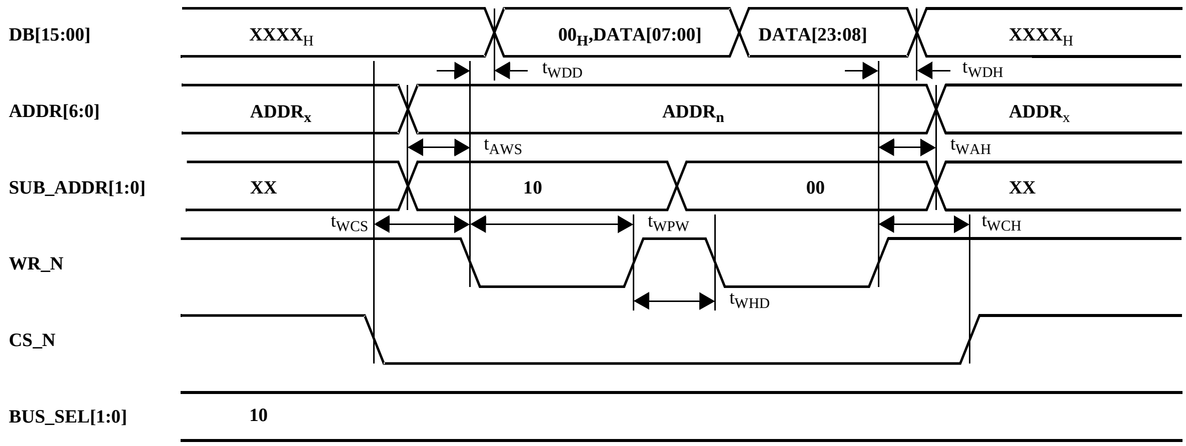


Figure 12: 16-Bit Data Bus Interface: Mode B

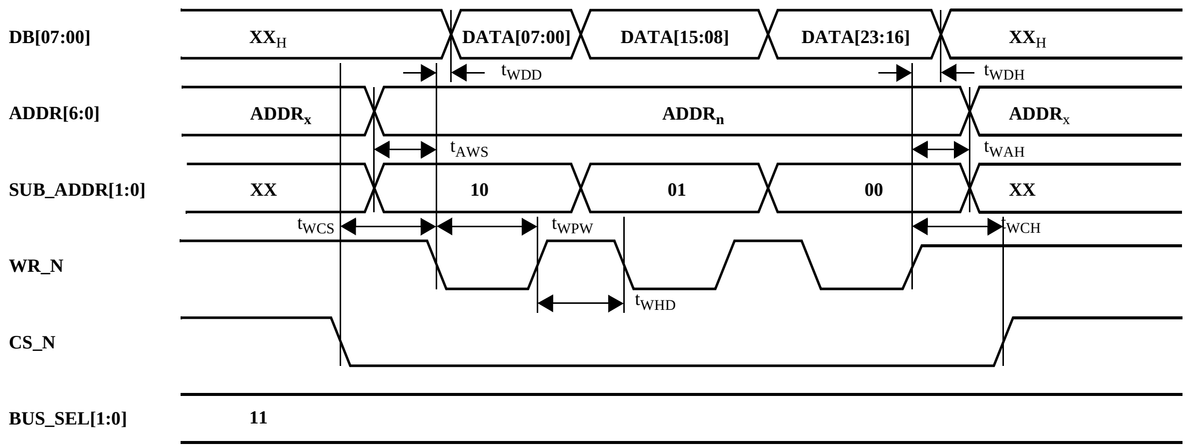


Figure 13: 8-Bit Data Bus Interface

Table 5: Write Cycle Timing Specifications $V_{CC} = 5.0V \pm 10\%$, $T_A = 0^o$ to $+70^oC$

Symbol	Parameter Description	Min	Max	Units
t_{WCS}	WR_N to CS_N Set Up	0		ns
t_{WCH}	WR_N to CS_N Hold	0		ns
t_{WPW}	WR_N Pulse Width	45		ns
t_{WHD}	WR_N High Delay	18		ns
t_{AWS}	ADDR to WR_N Set Up	0		ns
t_{WAH}	WR_N to ADDR Hold	0		ns

Table 5: Write Cycle Timing Specifications V_{CC} = 5.0V ± 10%, T_A = 0^o to $+70^oC$

Symbol	Parameter Description	Min	Max	Units
t_{WDD}	WR_N to Data Delay		25	ns
t_{WDH}	WR_N to Data Hold	0		ns

MACRO Interface

The MACROGATE chip provides a glue-less interface to the AMD TAXIchip™ chipset. Utilizing the TAXIchip™ chipset, it is easy to construct the high-speed communications network known as MACRO (Motion And Control Ring Optical).

Overview

MACRO is a communications standard for distributed machine control--both motion and I/O. It is a ring network, connecting a master controller to several slave nodes consisting of smart motor drives and I/O controllers. It provides high-frequency real-time communications between nodes for precision motion control and associated tasks.

Communications across the ring take place at a user-defined fixed frequency. Each ring communications cycle, all masters on the ring sequentially transmit command data to their corresponding slaves, and receive feedback data from these slaves. The masters always originate the communications; slaves can only respond to their master's communications by substituting their feedback data for their command data into the communications stream. Refer to the *MACRO Network Specifications Manual* for additional detail on the MACRO network.

The MACRO circuitry in the MACROGATE chip contains 16 nodes of read/write registers and two configuration registers. A single node consists of a 72-bit read only register, for receive data, and a 72-bit write only register, for transmit data. These 72-bit registers are internally sub-divided into four 24-bit/16-bit registers. See Global Register Map for byte alignment and addressing.

Configuration

The MACROGATE can be used for either Master Station or Slave Station functionality on a MACRO ring network. Bits 4 and 5 of the MACRO Status/Control register (17_H) determine the configuration.

Master Station

Each MACRO ring must have one, and only one, Ring Master. Its purpose is to start the ring communications cycle based upon its own internal timing circuits; for the Ring Master, this occurs on the rising edge of its Phase clock. For each ring communications cycle, the Ring Master sends out a data packet for each enabled node, followed by a Baton signal. This Baton signal is what allows a Master Station to 'hand off' control of the MACRO ring to another Master Station. A Master Station that is not configured as a Ring Master will not begin transmitting its own data until it receives the Baton signal. When it does receive the Baton signal, it sends out a data packet for each of its enabled nodes, followed by the Baton signal.

In a Master Station, the output registers (write only) contain command data written by the local station processor and are transmitted over the ring as command data packets. The input registers (read only) contain feedback data received over the MACRO ring from its Slave Stations, to be read by the local processor.

Slave Station

In a Slave Station, the output registers (write only) contain feedback data written by the local station processor and are transmitted over the ring as feedback data packets. The input registers (read only) contain command data received over the ring as command data packets from its associated Master Station, to be read by the local processor.

Node Addressing

Every node on each station has an 8-bit address number; 4 bits represent the Master Number and 4 bits represent the Node Number. The 4-bit Master Number is user programmed, while the 4-bit Node Number is hardwired for each of the sixteen available nodes in the MACROGATE. The MACRO ring communications take place between the active master nodes and the active slave nodes sharing the same address number. There may be only one active master node and one active slave node on the ring with any given address number. Since there are 256 possible address numbers, there may be 256 active master nodes and 256 active slave nodes on the ring at once. There is no limit, however, to the number of inactive nodes on the ring.

Bits [23:20] of the MACRO Node Enable register (16_H) determine the Master Number for the station (numbered 0 to 15). If the station is configured as a Master, this number is sent out as part of the address byte in each data packet. If the station is configured as a Slave, this number determines which Master Station's data will be accepted.

Bits [15:00] of the MACRO Node Enable register (16_H) determine which nodes of the sixteen available nodes (numbered 0 to 15) are enabled. Bit n controls node n. Setting a bit to one enables the node, while setting a bit to zero disables that node. These nodes are internally numbered in the MACROGATE with a 4-bit address known as the Node Number.

Bits [15:08] of the MACRO Status/Control register (17_H) determine the whether nodes #[15:08], respectively, check the Master Number of the incoming data packets. If the bit is set to 0, both the Master Number and the Node Number in the address byte must match for data to be accepted in that particular node. On the other hand, if the bit is set to 1, only the Node Number is checked for each of the nodes #08 to #15. Disabling of the Master Number checking allows a single master to broadcast a data packet to other Master Stations and other Slave Stations with different masters.

Synchronization

The MACROGATE provides a simple yet powerful method of synchronization between the stations on the MACRO ring. Bits [19:16] of the MACRO Node Enable register (16_H) specify the Node Number of the data packet that will create an internal sync signal in the MACROGATE chip. (The data packet's Master Number must still match the station's Master Number, or have its checking disabled).

The Sync Packet capability serves several important purposes. First, it ensures the tightest possible coordination between the axes. Second, it can be used to keep the clocks of different stations from 'walking' with respect to each other, which could possibly introduce a beat frequency. Third, it can prevent contention between register access from the ring and the local station processor, eliminating the need to double buffer the registers.

When the Sync Packet is received, the PWM up-down counter is forced to zero and a falling edge of the Phase clock is generated. For this function to be used properly, the Phase clock direction control bit in the Clock Control register ($1F_H$) must be set to zero or output mode. Using this function, multiple stations can be synchronized to a single Master Station.

Ring Status

The MACROGATE provides four status bits in the MACRO Status/Control register (17_H) to help in determining the operational status of the MACRO ring. Data packets with errors are not latched into the receive register. Each of the following status bits latches at 1 when an error occurs. Only the act of reading the MACRO Status/Control register will clear the bits.

Bit 0 indicates a 'Data Overflow Error'. If it is set to 1, a data packet was received with too many data bytes.

Bit 1 indicates a 'Byte Violation Error'. If it is set to 1, the TAXIchip™ chipset detected an error in transmission and set the TAXI_VLTN pin.

Bit 2 indicates a 'Packet Parity Error'. If it is set to 1, the MACROGATE detected a longitudinal parity error.

Bit 3 indicates a 'Data Underflow Error'. If it is set to 1, a data packet with too few data bytes was received.

Parity Generation

The MACROGATE generates a longitudinal parity byte for each data packet transmitted. Each bit of the parity byte is generated by checking the parity for all of the bits in that bit position for all nine data bytes. The parity bit is such that the overall parity is even. In other words, $P_n = D0_n + D1_n + D2_n + D3_n + D4_n + D5_n + D6_n + D7_n + D8_n$, where P is the parity byte, Dm is the data byte, and n is the bit position within each byte.

Baton Signal

The Master Stations use the Baton signal to transfer control of the MACRO ring to another Master Station. When each Master Station has completed transmission of all of its command/data packets, it appends the Baton signal to the end of its transmission. The Baton signal is simply the TAXI_COUT pin asserted high with two pulses on the TAXI_STROBEOUT pin.

Operational Modes

Table 6 below summarizes the three operational modes of each possible type of station on the MACRO ring network.

Table 6: MACRO Station Configurations

Station Type	MACRO configuration bits [5:4]	Initiates Ring Comm.	Transmits Data	Retransmits Data	Receives Data
Ring Master	11	Yes	On rising edge of Phase, all enabled nodes	If Master number of data packet does not match internal Master number, or if the node is disabled	If Master number of data packet matches internal Master number and the node is enabled
Reserved	10				
Master	01	No	Upon reception of the Baton signal, all enabled nodes	If Master number of data packet does not match internal Master number, or if the node is disabled	If Master number of data packet matches internal Master number and the node is enabled
Slave	00	No	If Master number of data packet matches internal Master number and the node is enabled	If Master number of data packet does not match internal Master number, or if the node is disabled	If Master number of data packet matches internal Master number and the node is enabled

MACRO Input Data Timing

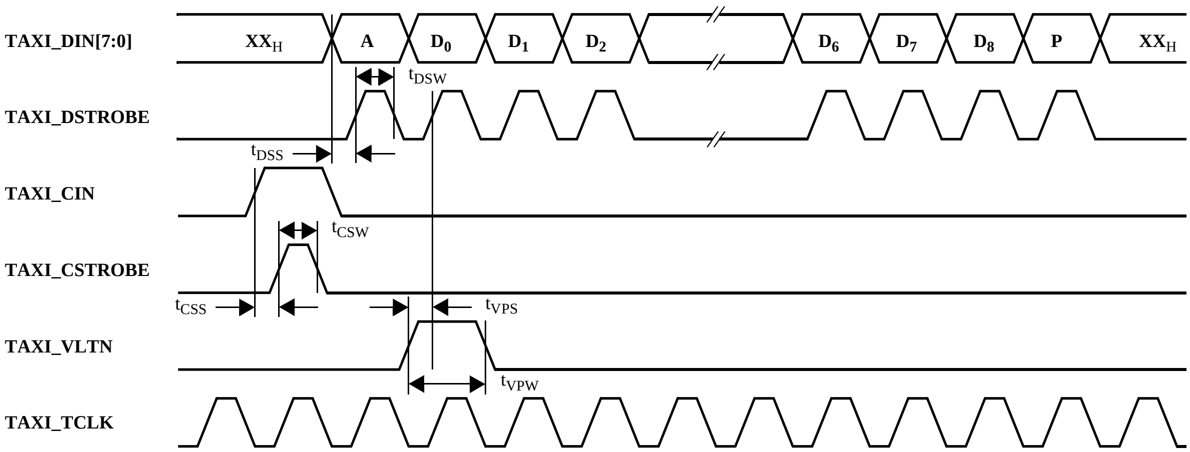


Figure 14: TAXIchip™ Interface Timing: Input Data

Table 7: MACRO Input Data Timing Specifications V_{CC} = 5.0V ± 10%, T_A = 0^o to +70^{o}C

Symbol	Parameter Description	Min	Max	Units
t_{DSS}	Data to Data Strobe Set Up	5		ns
t_{DSW}	Data Strobe Pulse Width	20		ns
t_{CSS}	Command to Command Strobe Set Up	5		ns
t_{CSS}	Command Strobe Pulse Width	20		ns
t_{VPS}	Violation Pulse to Data Strobe Set Up	5		ns
t_{VPW}	Violation Pulse Width	10		ns

Table 8: MACRO Input Data Description

Symbol	Description	Notes
A	Address Byte. Upper nibble of the address byte is the Master Number. Lower nibble of the address byte is the Node Number.	
$D_{[8:0]}$	Data Byte. D_0 is the least significant byte of the 72-bit data word. D_8 is the most significant byte.	
P	Parity Check Byte.	

MACRO Output Data Timing

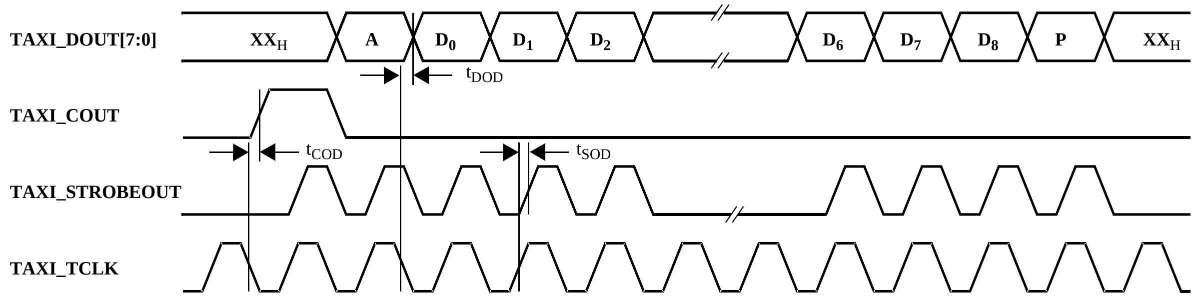


Figure 15: TAXIchip™ Interface Timing: Output Data

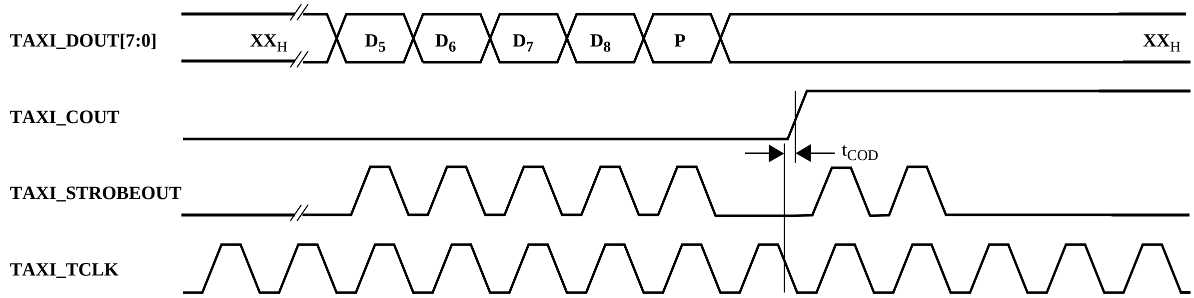


Figure 16: TAXIchip™ Interface Timing: Baton Signal

Table 9: MACRO Output Data Timing Specifications V_{CC} = 5.0V ± 10%, T_A = 0^o to +70^{o}C, C_{LOAD} = 50 pF

Symbol	Parameter Description	Min	Max	Units
t_{DOD}	Data Out Delay	7	24	ns
t_{COD}	Command Out Delay	6	17	ns
t_{SOD}	Strobe Out Delay	5	14	ns

Table 10: MACRO Output Data Description

Symbol	Description	Notes
A	Address Byte. Upper nibble of the address byte is the Master number. Lower nibble of the address byte is the node number.	
$D_{[8:0]}$	Data Byte. D_0 is the least significant byte of the 72-bit data word. D_8 is the most significant byte.	
P	Parity Check Byte.	

MACRO-to-MACRO Networking

The MACROGATE has the capability of connecting to another MACROGATE chip directly, in lieu of a ring network. For this mode to operate properly, any MACROGATE chip on the receiving side of a MACRO-to-MACRO connection must have its TAXI_MODE pin tied to +5 Volts. The connections are as follows:

- TAXI_DOUT[7:0] to TAXI_DIN[7:0]
- TAXI_COUT to TAXI_CIN
- TAXI_STROBEOUT to TAXI_CSTROBE
- TAXI_DSTROBE is grounded
- TAXI_VLTN is grounded

Figure 17 illustrates the connections.

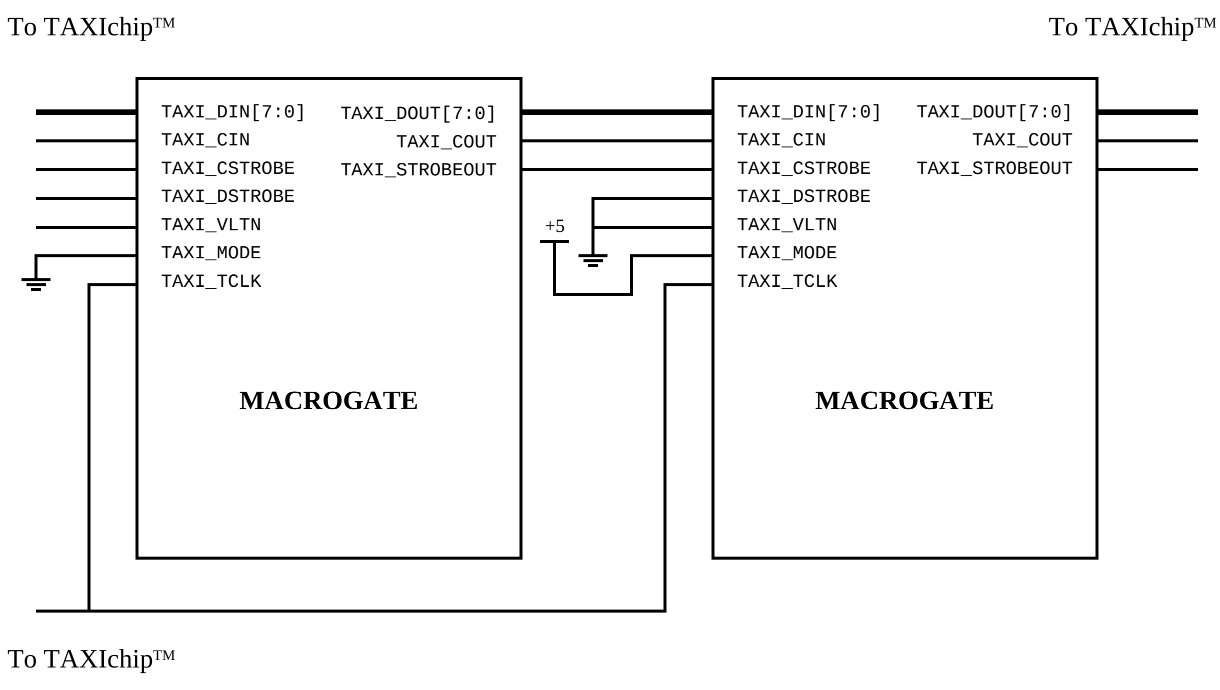


Figure 17: MACRO-to-MACRO Connectivity

Input/Output Port

The MACROGATE contains a 24-bit input port and a 24-bit output port. Both are accessible through the processor interface.

The 24-bit input port is latchable, with three separate latch controls for the three individual bytes within the 24 bits. The latches are transparent when the latch control pin is high, and data is latched when the control pin is low; latching occurs on the falling edge. The polarity of the latch control pin may be inverted by setting the ILATCH_INV pin high; setting this pin high reverses the polarity for all of the latch controls.

The 24 bits of read-only data is available at address 00_H. The read data is that of the latched data, so to monitor the status of the input pins, set the latch controls to be transparent.

The 24-bit output port is accessed through the 24-bit register at address 01_H. Any data written to this register is immediately driven at the output port.

Figure 18: 24-Bit Input Port Timing

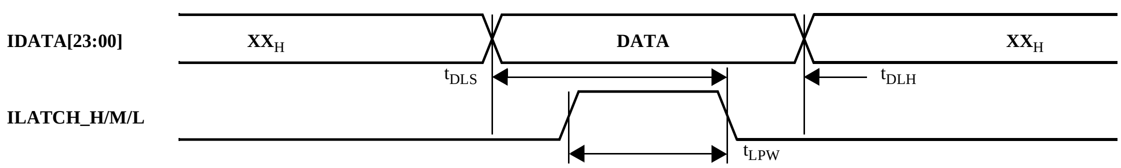


Table 11: 24-Bit Input Port Timing Specifications V_{CC} = 5.0V ± 10%, T_A = 0^o to +70^{o}C

Symbol	Parameter Description	Min	Max	Units
t_{DLS}	Data to Latch Set Up	5		ns
t_{DLH}	Data to Latch Hold	5		ns
t_{LPW}	Latch Pulse Width	10		ns

Quadrature Decoder

The two most significant bits of the 24-bit input port may be used as inputs to the A/B quadrature decoder. IDATA23 is the A input and IDATA22 is the B input to the quadrature decoder.

The A and B inputs to the quadrature decoder are first filtered through a simple digital delay filter. This filter is clocked by the internal sample clock, S_CLK, and is designed to remove pulses less than two clock cycles wide. The frequency of the sample clock is user selectable to suit the requirements of the A/B quadrature signals and any potential noise hazards. It is important to note that the sample clock frequency must be at least two times that of the A/B signals to pass through the digital filters.

The quadrature decoder operates on the rising and falling edges of the A/B inputs. The encoder counter increments or decrements by one count on each edge; the direction is determined by whether A or B is leading. Figure 19 illustrates the timing.

24-Bit Encoder Counter

The 24-bit encoder counter is a 24-bit up/down counter readable through the processor interface at address 29_H. A read operation of this address returns the current encoder count, while a write operation, clears the count to zero.

The counter does not saturate at the extremes, and rolls over at $FFFFFF_H$ and 000000_H.

Sample Clock

The sample clock, S_CLK, is generated by an internal 40 Mhz signal (PLLCLK x 2) through a divide-by-2^n circuit, where n = 0 to 7. The selection is user programmed with bits [2:0] in the Clock Control register at $1F_H$. For example, if bits [2:0] = 010_B, n = 2 and S_CLK = 10 Mhz (PLLCLK / 2).

Phase Clock

The MACROGATE generates the internal signal Phase clock for use as a master timing signal by the MACRO circuitry. For the Ring Master, all ring communications initiate on the rising edge of its Phase clock.

The Phase clock is generated by a 16-bit up/down counter. The limits of the counter is controlled by the Clock Control register at address $1F_H$. The counter counts in the positive direction until it reaches (MaxCount + 1). It then counts down until it reaches (-MaxCount - 2), at which time it begins counting up again. The Phase clock, then, is produced by detecting the zero crossings and max/min limits of this counter--the rising edge of the Phase clock occurs at the max/min limits, and the falling edge occurs at the zero crossings.

The Phase clock may be further divided down by a divide-by-(n+1) circuit, where n is a programmable value from 0 to 15. Bits [19:16] of the Clock Control register at address $1F_H$ determine the n value. The MACROGATE chip also has provisions for an external Phase clock. By setting bit 12 of the Clock Control register, the Phase pin is configured as an input; clearing bit 12 puts the Phase pin in output mode. If an external

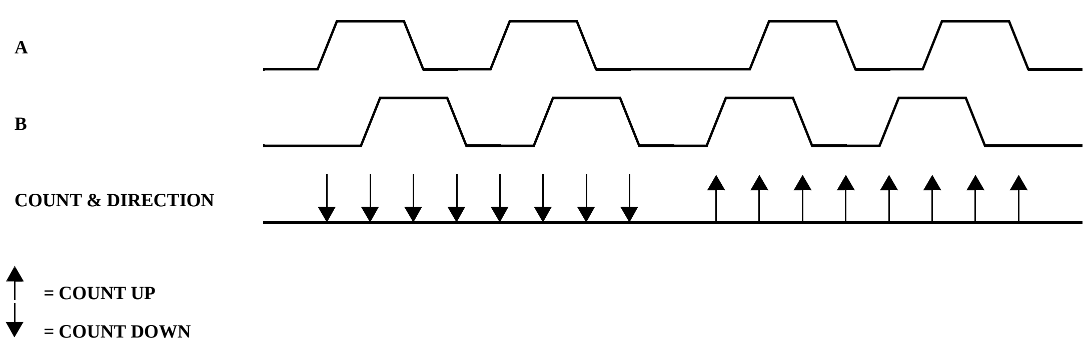


Figure 19: Quadrature Decoder Timing

Phase clock is used, the 16-bit up/down counter is forced to zero on the falling edge of the Phase clock. It is important that the internal Phase frequency be set as close as possible to an integer multiple of the external Phase frequency.

The versatility of the Phase clock direction allows a single master Phase clock to be used throughout the user's system. This master Phase clock may be used to synchronize all hardware and software processes. It may be used by all local MACROGATE devices or as a software interrupt for the local processor.

The Phase clock frequency may be calculated by Equation 1, below. For example, for a Phase frequency of 9 Khz, set MaxCount = 6527 (decimal) and n = 0.

$$Phase\ frequency = \frac{6 \times PLLCLK}{(2MaxCount + 3)(n + 1)}$$

Equation 1: Phase Frequency

Global Register Map

Table 12: MACROGATE Register Map

Address	Name	Bits	Description
00_H	Input Data	[23:00]	Latched data from the input pins IDATA[23:00]. The latching of the input data is controlled by ILATCH_x, where ILATCH_H is assigned to IDATA[23:16], ILATCH_M is assigned to IDATA[15:08], and ILATCH_L is assigned to IDATA[07:00]. The input latch is transparent when ILATCH_x = 1. Latching occurs on the falling edge of ILATCH_x. The polarity of these latch enables can be inverted by setting ILATCH_INV = 1.
01_H	Output Data	[23:00]	Output data mapped to the output pins ODATA[23:00].
02_H -15_H	Reserved	[23:00]	Reserved for future use.
16_H	MACRO Node Enable	[23:00]	Bit 00: Node 00 enable. (0=disable, 1=enable) Bit 01: Node 01 enable. ... Bit 15: Node 15 enable. Bits [19:16]: Sync Packet node number. Bits [23:20]: Master Number.
17_H	MACRO Status/Control	[15:00]	Bit 00: Data Overflow Error. (cleared on read) Bit 01: TAXI Violation Error. (cleared on read) Bit 02: Parity Error. (cleared on read) Bit 03: Data Underflow Error. (cleared on read) Bits [05:04]: MACRO Station Configuration. Bit 06: Sync Packet received. (cleared on read) Bit 07: Sync Packet phase lock enable. (0=disable, 1=enable) Bit 08: Node 08 Master Number check disable. (0=enable, 1=disable) Bit 09: Node 09 Master Number check disable. ... Bit 15: Node 15 Master Number check disable.

Table 12: MACROGATE Register Map

Address	Name	Bits	Description
18_H - $1E_H$	Reserved	[23:00]	Reserved for future use.
$1F_H$	Clock Control	[19:00]	Bits [19:16]: Phase clock divider. See Equation 1. Bits [15:13]: Not Used. Bit 12: Phase clock direction. (0=output, 1=input) Bits [11:03]: Not Used. Bits [02:00]: S_CLK clock divider. S_CLK = 40 Mhz / 2^n
20_H - 28_H	Reserved	[23:00]	Reserved for future use.
29_H	Encoder Count	[23:00]	Current count of the 24-bit encoder counter. Writing any value to this register clears the counter.
$2A_H$ - $3B_H$	Reserved	[23:00]	Reserved for future use.
$3C_H$	PWM Max-Count	[23:08]	PWM MaxCount value used to generate the Phase clock.
$3D_H$ - $3F_H$	Reserved	[23:00]	Reserved for future use.
40_H	MACRO Data Node #00A	[23:00]	MACRO Data word, node #00, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
41_H	MACRO Data Node #00B	[23:08]	MACRO Data word, node #00, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
42_H	MACRO Data Node #00C	[23:08]	MACRO Data word, node #00, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
43_H	MACRO Data Node #00D	[23:08]	MACRO Data word, node #00, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
44_H	MACRO Data Node #01A	[23:00]	MACRO Data word, node #01, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
45_H	MACR Data Node #01B	[23:08]	MACRO Data word, node #01, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
46_H	MACRO Data Node #01C	[23:08]	MACRO Data word, node #01, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
47_H	MACRO Data Node #01D	[23:08]	MACRO Data word, node #01, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
48_H	MACRO Data Node #02A	[23:00]	MACRO Data word, node #02, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
49_H	MACRO Data Node #02B	[23:08]	MACRO Data word, node #02, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.

Table 12: MACROGATE Register Map

Address	Name	Bits	Description
$4A_H$	MACRO Data Node #02C	[23:08]	MACRO Data word, node #02, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$4B_H$	MACRO Data Node #02D	[23:08]	MACRO Data word, node #02, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$4C_H$	MACRO Data Node #03A	[23:00]	MACRO Data word, node #03, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
$4D_H$	MACRO Data Node #03B	[23:08]	MACRO Data word, node #03, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$4E_H$	MACRO Data Node #03C	[23:08]	MACRO Data word, node #03, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$4F_H$	MACRO Data Node #03D	[23:08]	MACRO Data word, node #03, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
50_H	MACRO Data Node #04A	[23:00]	MACRO Data word, node #04, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
51_H	MACRO Data Node #04B	[23:08]	MACRO Data word, node #04, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
52_H	MACRO Data Node #04C	[23:08]	MACRO Data word, node #04, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
53_H	MACRO Data Node #04D	[23:08]	MACRO Data word, node #04, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
54_H	MACRO Data Node #05A	[23:00]	MACRO Data word, node #05, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
55_H	MACRO Data Node #05B	[23:08]	MACRO Data word, node #05, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
56_H	MACRO Data Node #05C	[23:08]	MACRO Data word, node #05, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
57_H	MACRO Data Node #05D	[23:08]	MACRO Data word, node #05, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
58_H	MACRO Data Node #06A	[23:00]	MACRO Data word, node #06, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.

Table 12: MACROGATE Register Map

Address	Name	Bits	Description
59_H	MACRO Data Node #06B	[23:08]	MACRO Data word, node #06, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$5A_H$	MACRO Data Node #06C	[23:08]	MACRO Data word, node #06, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$5B_H$	MACRO Data Node #06D	[23:08]	MACRO Data word, node #06, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$5C_H$	MACRO Data Node #07A	[23:00]	MACRO Data word, node #07, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
$5D_H$	MACRO Data Node #07B	[23:08]	MACRO Data word, node #07, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$5E_H$	MACRO Data Node #07C	[23:08]	MACRO Data word, node #07, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$5F_H$	MACRO Data Node #07D	[23:08]	MACRO Data word, node #07, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
60_H	MACRO Data Node #08A	[23:00]	MACRO Data word, node #08, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
61_H	MACRO Data Node #08B	[23:08]	MACRO Data word, node #08, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
62_H	MACRO Data Node #08C	[23:08]	MACRO Data word, node #08, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
63_H	MACRO Data Node #08D	[23:08]	MACRO Data word, node #08, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
64_H	MACRO Data Node #09A	[23:00]	MACRO Data word, node #09, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
65_H	MACRO Data Node #09B	[23:08]	MACRO Data word, node #09, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
66_H	MACRO Data Node #09C	[23:08]	MACRO Data word, node #09, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
67_H	MACRO Data Node #09D	[23:08]	MACRO Data word, node #09, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.

Table 12: MACROGATE Register Map

Address	Name	Bits	Description
68_H	MACRO Data Node #10A	[23:00]	MACRO Data word, node #10, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
69_H	MACRO Data Node #10B	[23:08]	MACRO Data word, node #10, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$6A_H$	MACRO Data Node #10C	[23:08]	MACRO Data word, node #10, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$6B_H$	MACRO Data Node #10D	[23:08]	MACRO Data word, node #10, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$6C_H$	MACRO Data Node #11A	[23:00]	MACRO Data word, node #11, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
$6D_H$	MACRO Data Node #11B	[23:08]	MACRO Data word, node #11, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$6E_H$	MACRO Data Node #11C	[23:08]	MACRO Data word, node #11, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$6F_H$	MACRO Data Node #11D	[23:08]	MACRO Data word, node #11, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
70_H	MACRO Data Node #12A	[23:00]	MACRO Data word, node #12, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
71_H	MACRO Data Node #12B	[23:08]	MACRO Data word, node #12, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
72_H	MACRO Data Node #12C	[23:08]	MACRO Data word, node #12, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
73_H	MACRO Data Node #12D	[23:08]	MACRO Data word, node #12, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
74_H	MACRO Data Node #13A	[23:00]	MACRO Data word, node #13, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
75_H	MACRO Data Node #13B	[23:08]	MACRO Data word, node #13, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
76_H	MACRO Data Node #13C	[23:08]	MACRO Data word, node #13, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.

Table 12: MACROGATE Register Map

Address	Name	Bits	Description
77_H	MACRO Data Node #13D	[23:08]	MACRO Data word, node #13, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
78_H	MACRO Data Node #14A	[23:00]	MACRO Data word, node #14, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
79_H	MACRO Data Node #14B	[23:08]	MACRO Data word, node #14, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$7A_H$	MACRO Data Node #14C	[23:08]	MACRO Data word, node #14, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$7B_H$	MACRO Data Node #14D	[23:08]	MACRO Data word, node #14, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$7C_H$	MACRO Data Node #15A	[23:00]	MACRO Data word, node #15, least significant 24 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data.
$7D_H$	MACRO Data Node #15B	[23:08]	MACRO Data word, node #15, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$7E_H$	MACRO Data Node #15C	[23:08]	MACRO Data word, node #15, middle significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.
$7F_H$	MACRO Data Node #15D	[23:08]	MACRO Data word, node #15, most significant 16 bits. Writing to this register, writes the MACRO transmit data. Reading this register, reads the MACRO receive data. Note: This register is left justified.

Appendix A.

Sample Circuit

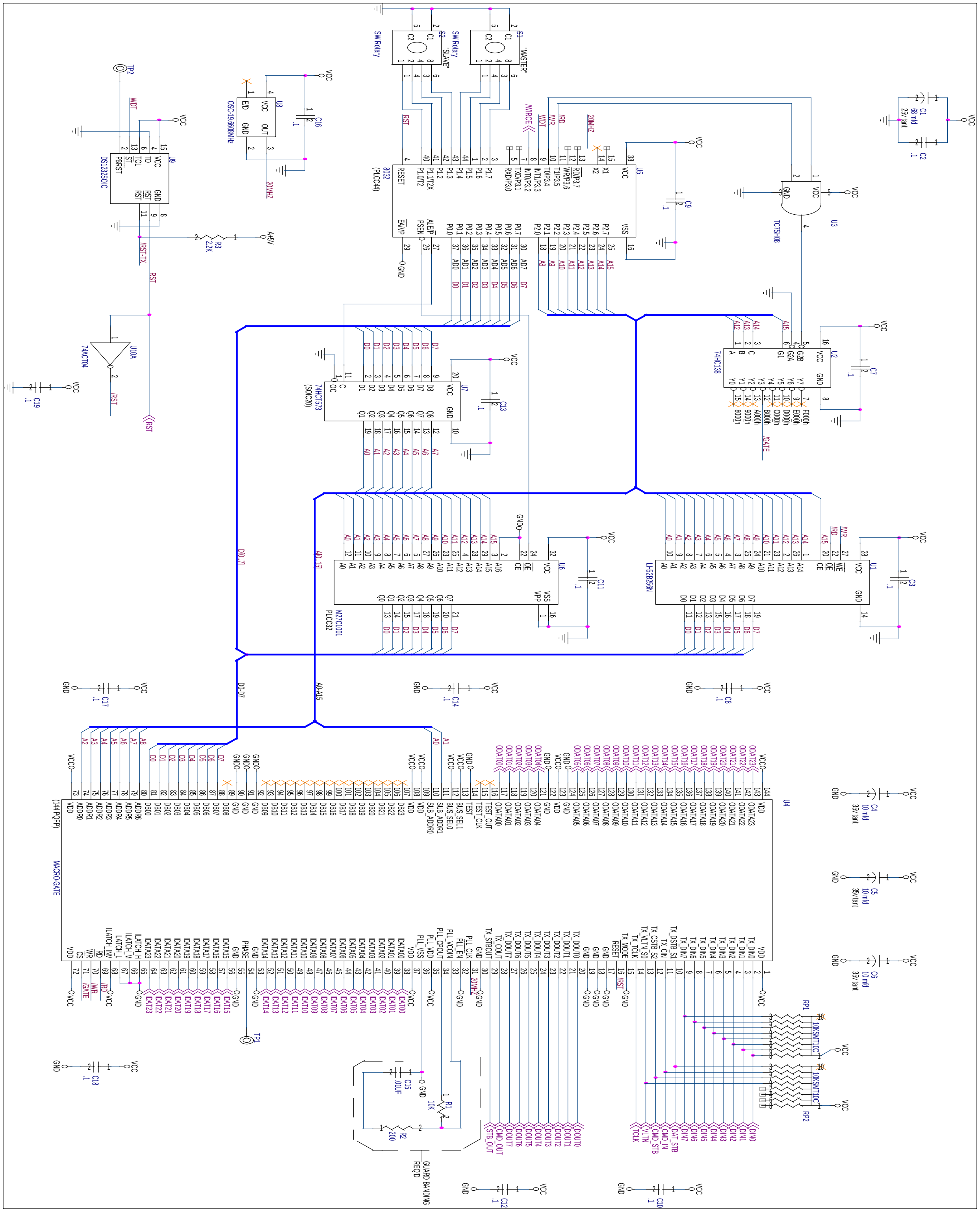


Figure A1: Sample Schematic: 8-bit Processor and MACROGATE

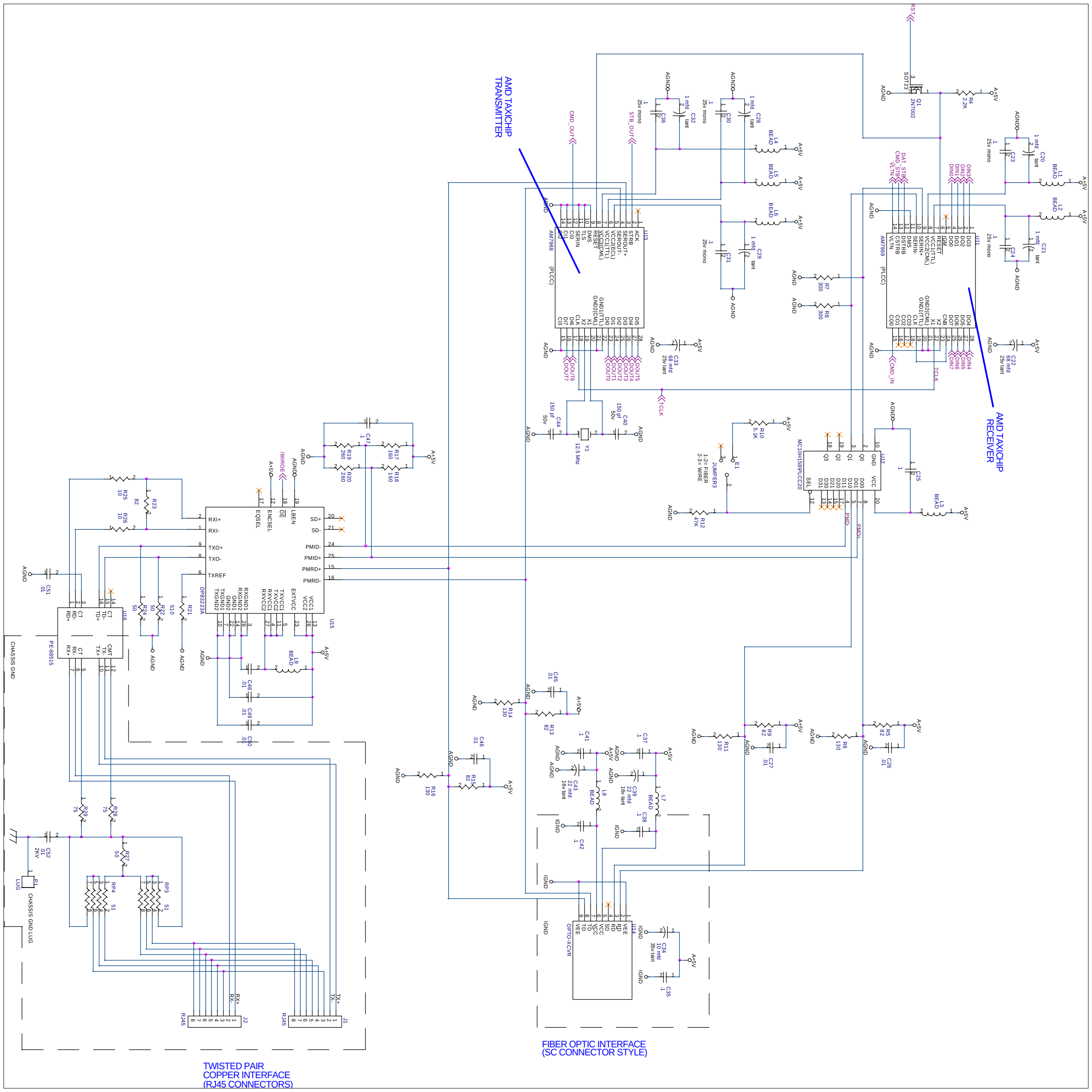


Figure A2: Sample Schematic: TAXIchip™ Interface

List of Materials

Table A1: List of Materials: 8-bit Sample Circuit

Item #	Quantity	Part	Reference Designator
1	3	68 uF	C1,C22,C33

Table A1: List of Materials: 8-bit Sample Circuit

Item #	Quantity	Part	Reference Designator
2	26	0.1 uF	C2,C3,C7,C8,C9,C10,C11,C12,C13, C14,C16,C17,C18,C19,C23, C24,C25,C30,C31,C35,C36,C37,C38, C41,C42,C47
3	4	10 uF	C4,C5,C6,C34
4	1	0.01 uF	C15
5	5	1 uF	C20,C21,C28,C29,C32
6	9	0.01 uF	C26,C27,C45,C46,C48,C49,C50,C51, C52
7	2	22 uF	C39,C43
8	2	150 pF	C40,C44
9	1	Jumper 3	E1
10	2	RJ45	J1,J2
11	9	Bead	L1,L2,L3,L4,L5,L6,L7,L8
12	1	Lug	P1
13	1	2N7002	Q1
14	2	10KSMT10C	RP1,RP2
15	2	51 Ω	RP3,RP4
16	1	10 kΩ	R1
17	1	200 Ω	R2
18	2	2.2k Ω	R3,R4
19	5	82 Ω	R5,R9,R13,R15,R23
20	4	130 Ω	R6,R11,R14,R16
21	2	300 Ω	R7,R8
22	1	5.1k Ω	R10
23	1	47k Ω	R12
24	2	160 Ω	R17,R18
25	2	260 Ω	R19,R20
26	1	510 Ω	R21
27	3	50 Ω	R22,R24,R27
28	2	10 Ω	R25,R26
29	2	75 Ω	R28,R29
30	2	SW Rotary	S1,S2
31	2	TP	TP1,TP2
32	1	LH52B256N	U1

Table A1: List of Materials: 8-bit Sample Circuit

Item #	Quantity	Part	Reference Designator
33	1	74HCT138	U2
34	1	TC7SH08	U3
35	1	MACROGATE	U4
36	1	8032	U5
37	1	M27C1001	U6
38	1	74HCT573	U7
39	1	OSC-19.6608 Mhz	U8
40	1	DS1232SOIC	U9
41	1	74ACT04	U10
42	1	AM7969	U11
43	1	MC10H158\PLCC20	U12
44	1	AM7968	U13
45	1	OPTO-XCVR	U14
46	1	DP83223A	U15
47	1	PE-68515	U16
48	1	12.5 Mhz	Y1